JW5716

Ultra-Low Quiescent Current Synchronous Step-Down Converter

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW®5716 provides an ultra-low power solution for products powered by either one rechargeable Li-Ion batteries, Li-primary battery chemistries such as $Li\text{-}MnO_2$ or two to three cell alkaline batteries. The output voltage of the buck converter is set with three VSEL pins between 0.7V and 3.3V. JW5716 features low output ripple voltage and low noise with a small output capacitor. Once the input voltage comes close to the output voltage the device enters the 100% duty cycle operation mode to prevent an increase of output ripple voltage. In this operation mode the device stops switching and turns the high-side MOSFET switch on.

JW5716 is available in DFN3X2-12 package, which provide a compact solution with minimal external components.

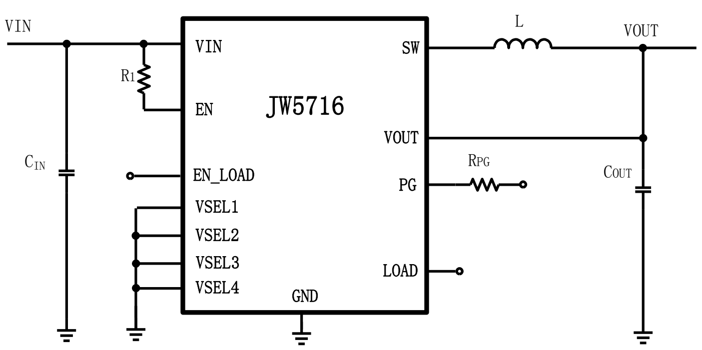
FEATURES

- 2.3V to 5.5V operating input range
- Output current
  JW5716: 300mA, peak to 400mA
- Typical 360nA quiescent current
- Up to 90% efficiency with load current>15uA
- Low output ripple voltage
- 8 selectable output voltages
  JW5716: 0.7V to 3.3V
- Output short protection
- Output voltage discharge
- Automatic transition to 100% duty cycle operation
- Thermal protection
- Available in DFN3X2-12 package

APPLICATIONS

- IOT
- Wearable and Personal Electronics
- Health Monitoring and Medical Accessories
- Industrial Metering
- Energy Harvesting

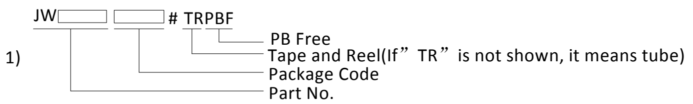
TYPICAL APPLICATION

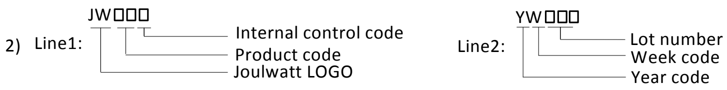


ORDER INFORMATION

DEVICE[1)	PACKAGE	TOP MARKING[2)
JW5716DFNP#TRPBF	DFN3x2-12	JWMJ□ YW□□□

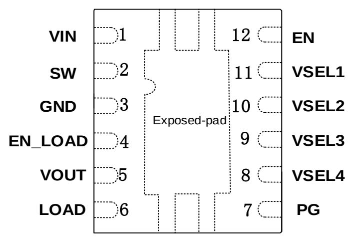
Note：





PIN CONFIGURATION

Top View



DFN3mmX2mm

ABSOLUTE MAXIMUM RATING[1)]

VIN, SW Pins .... -0.3V to 6V
All other Pins .... -0.3V to 6V
Junction Temperature[2)] 150ºC
Lead Temperature 260ºC
Storage Temperature .... -65ºC to +150ºC
ESD (HBM) ....±2kV
ESD (CDM) ....±500V

RECOMMENDED OPERATING CONDITIONS[3)]

Input Voltage VIN .... 2.3V to 5.5V
Output Current IOUT..300mA
Junction Temperature Range ....-40ºC to 125ºC

THERMAL PERFORMANCE[4)] θ_{JA} θ_{Jctop}

DFN3X2-12 ....61....7.2ºC/W

Note:

1. **1)** Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.
2. **2)** The JW5716 includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.
3. **3)** The device is not guaranteed to function outside of its operating conditions.
4. **4)** Measured on JESD51-7, 4-layer PCB

ELECTRICAL CHARACTERISTICS

VIN=3.6V, T_A= -40℃ to 85℃, typical values are at T_A= 25℃, Unless otherwise stated。						
Item	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{IN} Under-voltage Lockout Threshold	V_{IN_MIN}	V_{IN} rising		2.18	2.29	V
V_{IN} Under-voltage Lockout Hysteresis	$V_{IN\_MIN\_HYST}$			100		mV
Shutdown Supply Current	I_{SD}	V_{EN}=0V		100	300	nA
Supply Current	I_Q	device not switching		360	600	nA
		device switching[5)]		460	800	nA
High Side MOSFET On-resistance	$R_{DS(ON)T}$	V_{IN}=3.6V, I_{OUT}=50mA		380		mΩ
Low Side MOSFET On-resistance	$R_{DS(ON)B}$	V_{IN}=3.6V, I_{OUT}=50mA		250		mΩ
High Side MOSFET Switch Current Limit	I_{LIM_Peak}	3V≤V_{IN}≤5.5V	0.6	0.7	0.8	A
Low Side MOSFET Switch Current Limit	I_{LIM_Valley}	3V≤V_{IN}≤5.5V	0.4	0.5	0.6	A
Output Discharge Resistance	R_{DISCH}	EN=GND, I_{VOS}=-10mA into VOS pin		30	65	Ω
Load Switch On-resistance	R_{DSON_LOAD}	V_{OUT}=2V	0.3	0.5	0.7	Ω
Load Switch Discharge Resistance	R_{LOAD_DISCH}			35	65	Ω
Bias Current Into VOS Pin	I_{IN_VOS}	V_{OUT}=2V, EN=V_{IN}		100	200	nA
Output Voltage Accuracy	V_{OUT}	V_{OUT}=1.8V	-2		2	%
Output Voltage Load Regulation[5)]		V_{OUT}=1.8V		0.008		%/mA
Output Voltage Line Regulation[5)]		V_{OUT}=1.8V, I_{OUT}=100mA, 2.3V≤V_{IN}≤5.5V		0.12		%/V
Power Good Threshold Voltage	V_{TH_PG}	Rising output voltage on VOUT pin		98		%
Power Good Threshold Hysteresis	$V_{TH\_PG\_HYS}$			3.3		%
Power Good Sink Current	I_{PG}	V_{PG}=0.4V	10			mA
Minimum On Time	T_{ON_MIN}	I_{OUT}=0mA, V_{OUT}=2V		500		ns
Minimum Off Time	T_{OFF_MIN}	V_{IN}=2.3V		80		ns
Soft-start Delay Time	T_{SS_DLY}	From EN=low to high until device starts switching		10		ms
Soft-start Time[5)]	T_{SS}	2.3V≤V_{IN}≤5.5V, EN=V_{IN}		760		us
High Side MOSFET Switch Current Limit During Soft-start[5)]	$I_{LIM\_Peak\_SS}$	EN=low to high		330		mA

VIN=3.6V, T_A= -40℃ to 85℃, typical values are at T_A= 25℃, Unless otherwise stated。						
Item	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Low Side MOSFET Switch Current Limit During Soft-start[5)]	$I_{LIM\_Valley\_SS}$	EN=low to high		135		mA
Input High Threshold	V_{IH}	2.3V≤V_{IN}≤5.5V, EN, VSELs pins	1.2			V
Input Low Threshold	V_{IL}	2.3V ≤V_{IN}≤5.5V, EN, VSELs pins			0.4	V
Input Pin Bias Current	I_{IN}			10		nA
Auto 100% Mode Leave Detection Threshold	V_{TH_100+}	Rising V_{IN}, 100% mode is left with V_{IN}=V_{OUT}+V_{TH_100+}	200	320	440	mV
Auto 100% Mode Enter Detection Threshold	V_{TH_100-}	Falling V_{IN}, 100% mode is entered with V_{IN}=V_{OUT}+V_{TH_100-}	140	260	380	mV
Thermal Shutdown[5)]	T_{TSD}			150		° C
Thermal Shutdown Hysteresis[5)]	T_{TSD_HYST}			20		° C

Note:

5) Guaranteed by design.

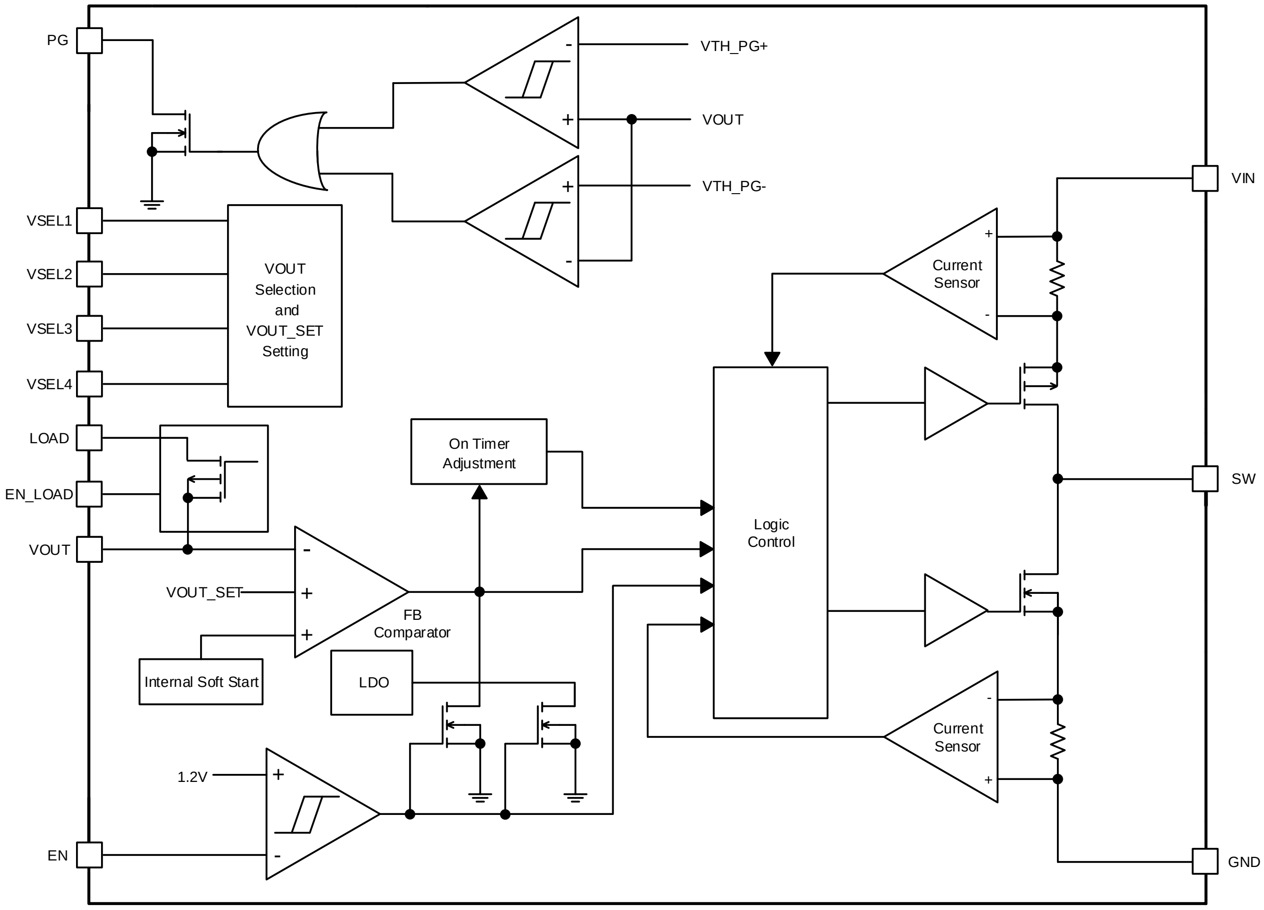
Table 1. Output Voltage Setting

VOUT/V	VSEL4	VSEL3	VSEL2	VSEL1
0.7	0	0	0	0
0.8	0	0	0	1
1.3	0	0	1	0
0.75	0	0	1	1
1.8	0	1	0	0
1.05	0	1	0	1
2.9	0	1	1	0
3.3	0	1	1	1

PIN DESCRIPTION

Pin	Name	Description
1	VIN	VIN power supply pin. Connect this pin close to the VIN terminal of the input capacitor. A ceramic capacitor of 4.7μF from this pin to GND is required.
2	SW	Switch pin which is connected to the internal MOSFET switches. Connect inductor to this terminal.
3	GND	Ground pin.
4	EN_LOAD	This pin connects / disconnects the internal load switch from VOUT to LOAD. With EN_LOAD = low, the switch is open. With EN_LOAD= high, the switch is closed connecting VOUT with LOAD. If not used, the pin should be tied to GND.
5	VOUT	Feedback pin for the internal feedback divider network and regulation loop. Connect this pin directly to the output capacitor with a short trace.
6	LOAD	Output of load switch connecting VOUT to LOAD when EN_LOAD=high. If not used, leave this pin open.
7	PG	This is an open drain power good output.
8	VSEL4	Output voltage selection pins.
9	VSEL3	
10	VSEL2	
11	VSEL1	
12	EN	Enable pin. Drive EN pin high to turn on the regulator and low to turn off the regulator.
Exposed-pad		Not electrically connected to the IC, but must be soldered. Connect this pad to GND and use it as a central thermal pad GND plane.

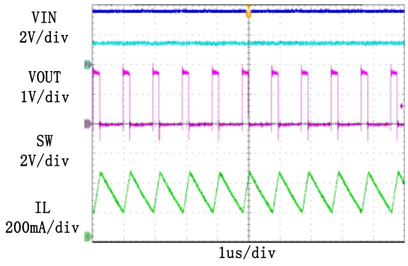
BLOCK DIAGRAM



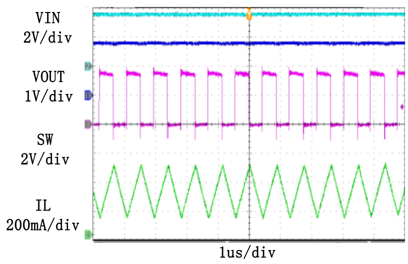
TYPICAL PERFORMANCE CHARACTERISTICS

VIN = 3.6V/4V, VOUT = 0.7V/1.8V/3.3V, L = 2.2μH, C_{OUT} = 10μF, T_A = +25°C, unless otherwise noted.

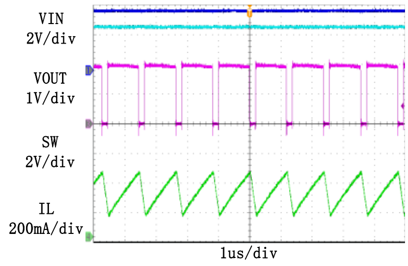
Steady State Test
VIN=3.6V, VOUT=0.7V
IOUT=300mA



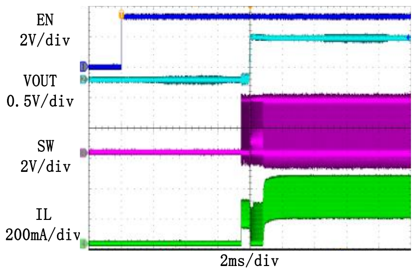
Steady State Test
VIN=3.6V, VOUT=1.8V
IOUT=300mA



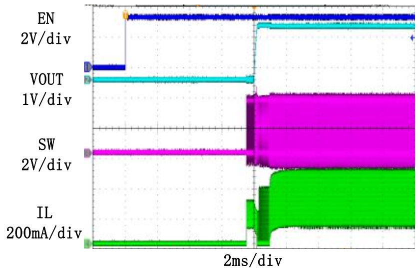
Steady State Test
VIN=4V, VOUT=3.3V
IOUT=300mA



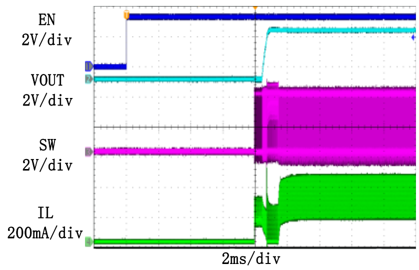
Startup through Enable
VIN=3.6V, VOUT=0.7V
IOUT=300mA (Resistive load)



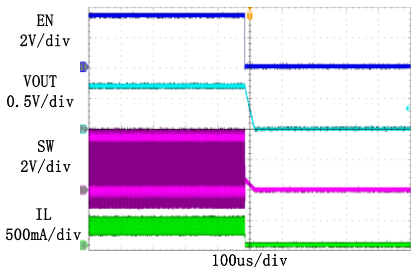
Startup through Enable
VIN=3.6V, VOUT=1.8V
IOUT=300mA (Resistive load)



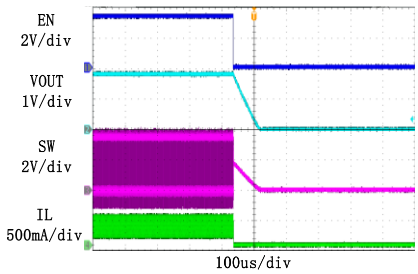
Startup through Enable
VIN=4V, VOUT=3.3V
IOUT=300mA (Resistive load)



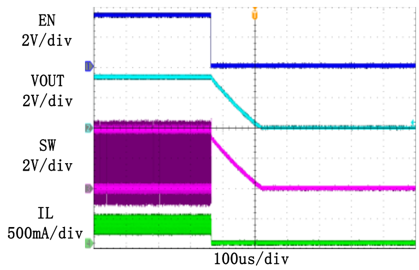
Shutdown through Enable
VIN=3.6V, VOUT=0.7V
IOUT=300mA (Resistive load)



Shutdown through Enable
VIN=3.6V, VOUT=1.8V
IOUT=300mA (Resistive load)



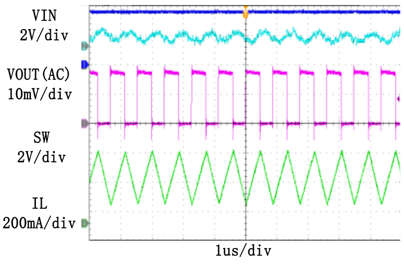
Shutdown through Enable
VIN=4V, VOUT=3.3V
IOUT=300mA (Resistive load)



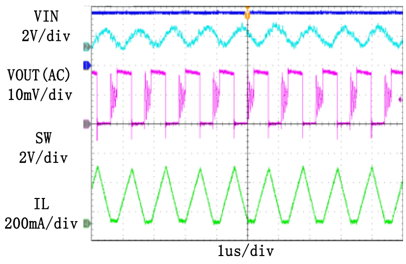
TYPICAL PERFORMANCE CHARACTERISTICS

VIN = 3.6V/4V, VOUT = 0.7V/1.8V/3.3V, L = 2.2μH, C_{OUT} = 10μF, T_A = +25°C, unless otherwise noted.

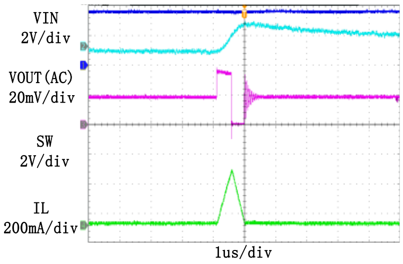
Heavy Load Operation
VIN=3.6V, VOUT=1.8V
IOUT=300mA



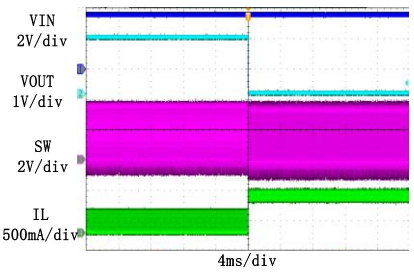
Light Load Operation
VIN=3.6V, VOUT=1.8V
IOUT=150mA



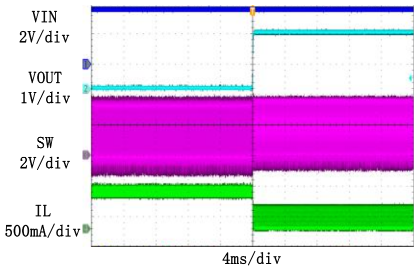
No Load Operation
VIN=3.6V, VOUT=1.8V
IOUT=0mA



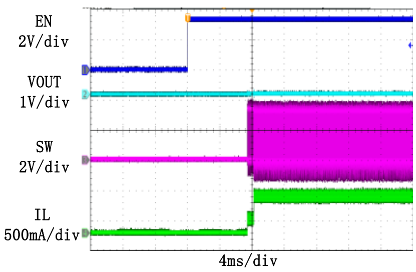
Short Circuit Protection
VIN=3.6V, VOUT=1.8V
IOUT=100mA- Short



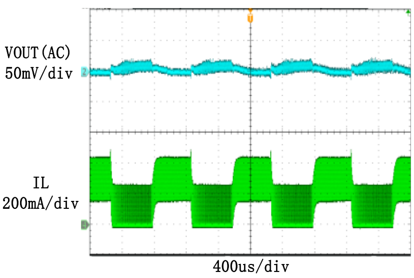
Short Circuit Recovery
VIN=3.6V, VOUT=1.8V
IOUT=Short-100mA



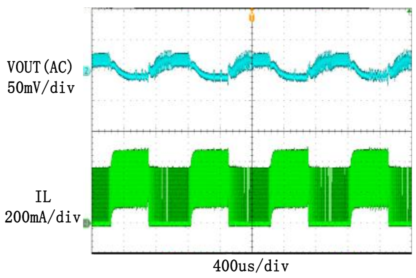
Short Circuit EN ON
VIN=3.6V, IOUT=Short



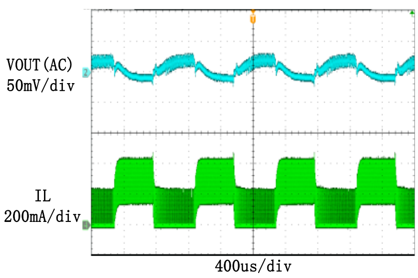
Load Transient
VIN=3.6V, VOUT=0.7V
30mA LOAD→300mA LOAD→30mA LOAD



Load Transient
VIN=3.6V, VOUT=1.8V
30mA LOAD→300mA LOAD→30mA LOAD



Load Transient
VIN=4V, VOUT=3.3V
30mA LOAD→300mA LOAD→30mA LOAD

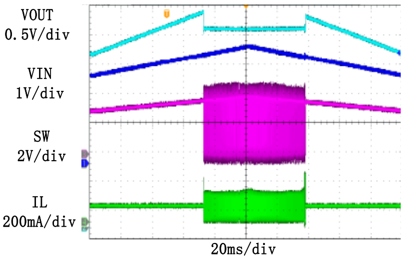


TYPICAL PERFORMANCE CHARACTERISTICS

VIN = 3.6V/4V, VOUT = 0.7V/1.8V/3.3V, L = 2.2μH, C_{OUT} = 10μF, T_A = +25°C, unless otherwise noted.

Automatic 100% Mode Transition

VIN=3V to 4V, VOUT=3.3V
IOUT=100mA



TYPICAL PERFORMANCE CHARACTERISTICS

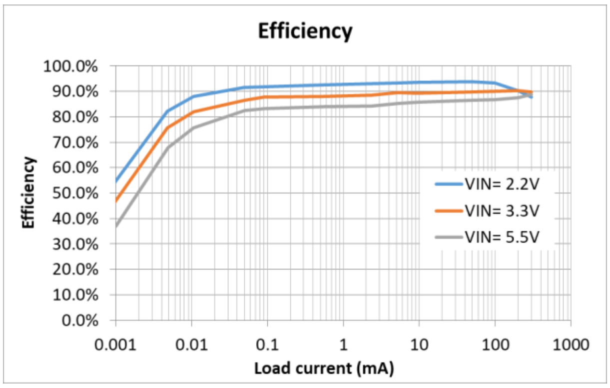


Figure 1. Efficiency vs. Load Current

(VOUT=1.8V, L=2.2μH)

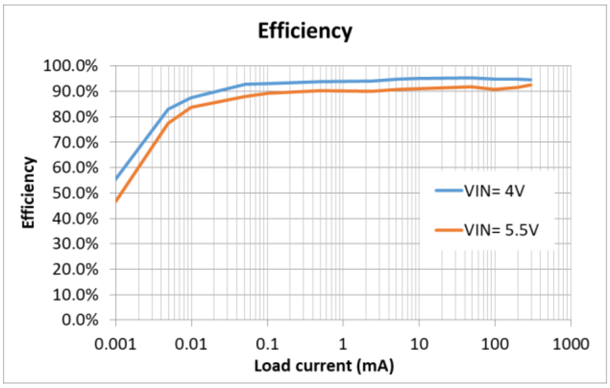


Figure 2. Efficiency vs. Load Current

(VOUT=3.3V, L=2.2μH)

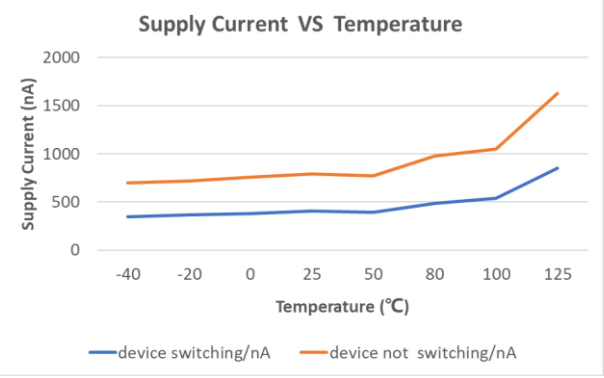


Figure 3. Supply Current vs. Junction Temperature

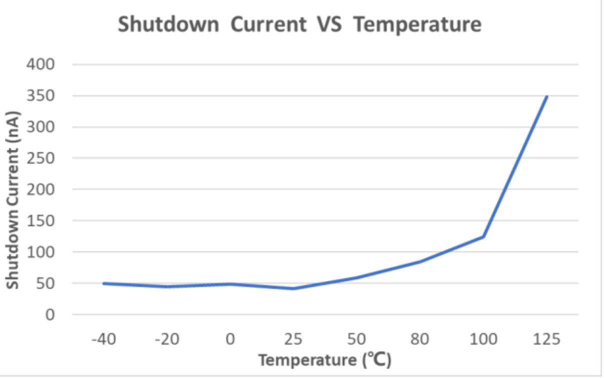


Figure 4. Shutdown Current vs. Junction Temperature

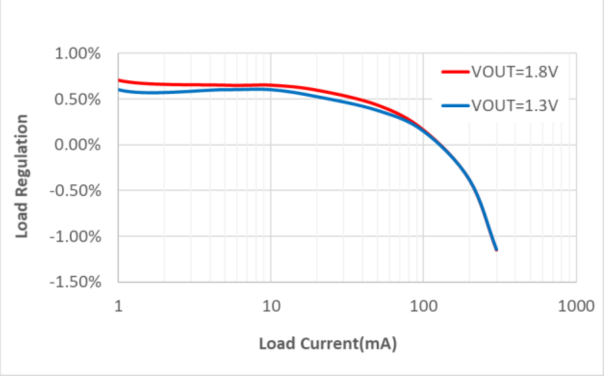


Figure 5. Load Regulation vs. Load Current

(VIN=5V, L=2.2μH)

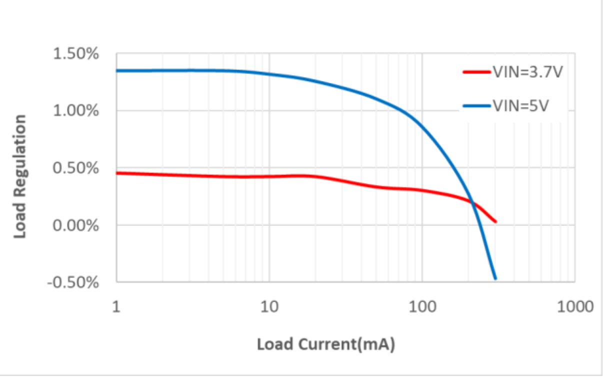


Figure 6. Load Regulation vs. Load Current

(VOUT=3.3V, L=2.2μH)

TYPICAL PERFORMANCE CHARACTERISTICS

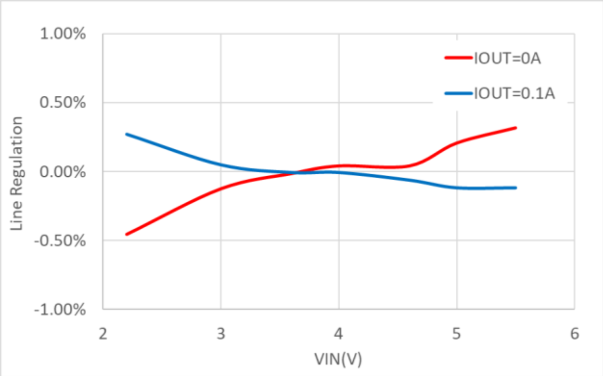


Figure 7. Line Regulation vs. Input Voltage

(VOUT=1.8V, L=2.2μH)

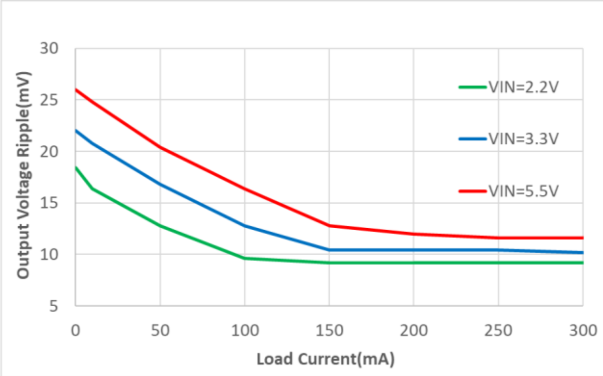


Figure 8. VOUT Ripple Voltage vs. Load Current

(VOUT=1.3V, L=2.2μH)

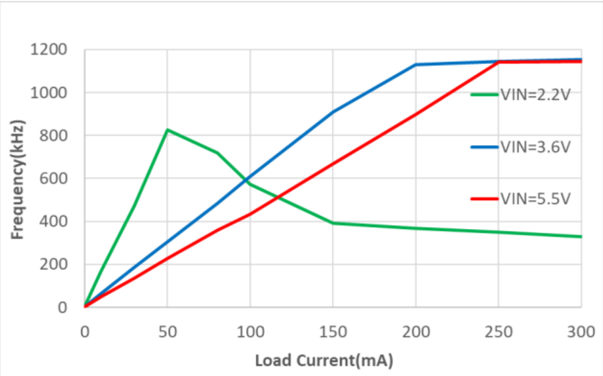


Figure9. Frequency vs. Load Current

(VOUT=1.8V, L=2.2μH)

FUNCTIONAL DESCRIPTION

JW5716 is an ultra-low power synchronous step-down regulator. It regulates input voltages from 2.3V to 5.5V down to an output voltage range from 0.7V to 3.3V with ultra low quiescent current consumption (360nA typical) and is capable of supplying to 300mA of continue load current and 400mA of peak load current.

Shut-Down Mode

JW5716 shuts down when voltage at EN pin is driven below 0.3V. The entire regulator is off and the supply current consumed by JW5716 drops below 300nA (100nA typical).

Enable and Adjustable UVLO Protection

The JW5716 is enabled when the VIN pin voltage rises above 2.18V and the EN pin voltage exceeds the enable threshold of 0.97V. The JW5716 is disabled when the VIN pin voltage falls below 2.08V or when the EN pin voltage is below 0.75V.

If an application requires a higher VIN under-voltage lockout (UVLO) threshold, use a resistive divider connected between VIN and ground with the central tap connected to EN to adjust the input voltage UVLO. (Shown in Figure 10). So that when VIN rises to the pre-set value, EN rises above 0.97V to enable the device and when VIN drops below the pre-set value, EN drops below 0.75V to trigger input under voltage lockout protection.

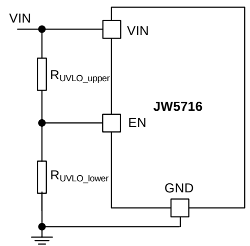


Figure 10. Adjustable UVLO

The input voltage UVLO threshold (V_{UVLO}) and hysteresis (V_{UVLO_HYS}) can be calculated by the following equation.

$$V_{UVLO} = \frac{R_{UVLO\_upper} + R_{UVLO\_lower}}{R_{UVLO\_lower}} \times V_{EN\_TH}$$

$$V_{UVLO\_HYS} = \frac{R_{UVLO\_upper} + R_{UVLO\_lower}}{R_{UVLO\_lower}} \times V_{EN\_HYS}$$

where

V_{EN_TH} is enable shutdown threshold (0.97V typ.);

V_{EN_HYS} is enable shutdown hysteresis (220mV typ.);

Output Voltage Selection

JW5716 does not require an external resistor divider network to program the output voltage. The device integrates a high impedance feedback resistor divider network which is programmed by VSEL1-4 pins. JW5716 supports an output voltage ranges of 0.7V to 3.3V. The output voltage can be changed during operation and supports simple dynamic output voltage scaling. The output voltage is programmed according to **Table 1**.

Soft Start

The JW5716 has an internal soft-start function to minimize input voltage drop during start-up. This allows the operation from high impedance battery cells. Once the device is enabled the device starts switching after a typical delay time of 10ms, then the soft-start time of typical 760μs begins with a reduced current limit of typical 330 mA. When this time passed by the device enters full current limit operation. This allows a smooth start-up and the device can start into full load current. Furthermore, larger output capacitors impact the start-up behavior of the DC/DC converter especially when the output voltage does not reach its nominal value after the typical soft-start time of 760μs has passed.

Power Good Indicator

The JW5716 has power-good (PG) output. The PG pin is the open drain of a MOSFET. Connect to VOUT or another voltage source through a resistor. When the output voltage becomes within -2% of the target value, internal comparators detect power good state and the power good signal becomes high. If the output voltage goes under 5.3% of the target value, the power good signal becomes low. The power good signal is as well as pulled to low level in case the input voltage falls below the under-voltage threshold or the device is disabled with EN=low. PG will be triggered when an output voltage change is ongoing due to a change in VSEL pin levels if the new target is high enough to trigger the PG threshold.

Output Current Run-Away Protection

JW5716 ingrates a current limit on the high side as well on the low side MOSFETs to protect the device against overload or short circuit conditions. The peak current in the switches is monitored cycle by cycle. If the high side MOSFET current limit is reached, the high side MOSFET is turned off and the low side MOSFET is turned on until the current decreases below the low side MOSFET current limit.

Output Discharge

The device provides automatic output voltage discharge once it is disabled. This feature prevents residual charge voltage on the output capacitor, which may impact proper power up of the system connected to the converter. The discharge circuit at VOS pin becomes active once the EN pin is pulled to low or the input voltage drops below UVLO comparator threshold.

Load Switch

The JW5716 integrates a 100mA load switch. The load switch connects VOUT pin to the LOAD pin and the on-resistance depends on the output voltage. At 2V VOUT, the on resistance is maximum 0.7Ω. The load switch can be used to power a sub-system controlled by EN_LOAD pin. To avoid a voltage drop at the output of the buck converter the load switch has an internal soft-start. With EN_LOAD=low the load switch is turned off and the LOAD pin is internally discharged to GND by typically 35Ω. This makes sure the output of the load switch is always discharged to GND before the load switch is turned on again.

100% Duty Cycle Operation Mode

Once the input voltage comes close to the output voltage, the DC/DC converter stops switching and enters 100% duty cycle operation mode and the output voltage VOUT tracks the input voltage VIN. Once the input voltage VIN falls below the 100% mode enter threshold, V_{TH_100-}, the DC/DC regulator is turned off, switching stops and therefore no output voltage ripple is generated. The voltage difference between VIN and VOUT is the voltage drop across the power inductor and the internal high side MOSFET switch. Once the input voltage increases and trips the 100% mode exit threshold, V_{TH_100+} , the DC/DC regulator turns on and starts switching again.

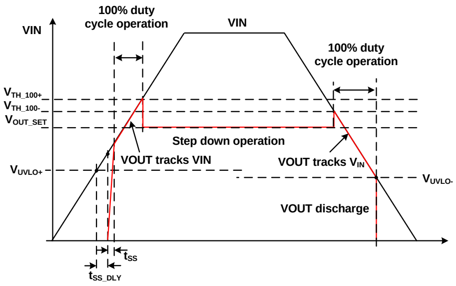


Figure 11. Automatic 100% Mode Transition

Thermal Protection

When the temperature of the JW5716 rises above 150°C, it is forced into thermal shut-down. Only when core temperature drops below 130°C can the regulator become active again.

APPLICATION INFORMATION

Input Capacitor

The input capacitor is used to supply the AC input current to the step-down converter and maintaining the DC input voltage. The ripple current through the input capacitor can be calculated by:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

where I_{OUT} is the load current, V_{OUT} is the output voltage, V_{IN} is the input voltage.

Thus, the input capacitor can be calculated by the following equation when the input ripple voltage is determined.

$$C_{IN} = \frac{I_{OUT}}{f_S \times \Delta V_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where C_{IN} is the input capacitance value, f_S is the switching frequency, $\triangle V_{IN}$ is the input ripple current.

The input capacitor can be electrolytic, tantalum or ceramic. To minimizing the potential noise, a small X5R or X7R ceramic capacitor, i.e. 0.1uF, should be placed as close to the IC as possible when using electrolytic capacitors.

A 4.7uF ceramic capacitor is recommended in typical application, and an extra 47uF electrolytic capacitor is needed if hot-plug is required.

Output Capacitor

The output capacitor is required to maintain the DC output voltage, and the capacitance value determines the output ripple voltage. The output voltage ripple can be calculated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C_{OUT}}\right)$$

where C_{OUT} is the output capacitance value and R_{ESR} is the equivalent series resistance value of the output capacitor.

The output capacitor can be low ESR electrolytic, tantalum or ceramic, which lower ESR capacitors get lower output ripple voltage.

The output capacitors also affect the system stability and transient response, and a 10uF ceramic capacitor is recommended in typical application.

Inductor

The recommended power inductor is 2.2uH and inductor saturation current rating choose follow over current protection design consideration. In applications, it needs to select an inductor with the low DCR to provide good performance and efficiency.

Power Good

The JW5716 has power-good (PG) output. The PG pin is the open drain of a MOSFET. Connect to V_{OUT} or another voltage source through a resistor.

JoulWatt recommends using R_{PG} from the values of 10kΩ to 100kΩ.

PCB Layout Note

For minimum noise problem and best operating performance, the PCB is preferred to following the guidelines as reference.

1.Place the input decoupling capacitor as close to JW5716 (V_{IN} pin and GND) as possible to eliminate noise at the input pin. The loop area formed by input capacitor and GND must be minimized.

2. Keep the switching node SW short to prevent excessive capacitive coupling

3. Make V_{IN}, V_{OUT} and ground bus connections as wide as possible. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.

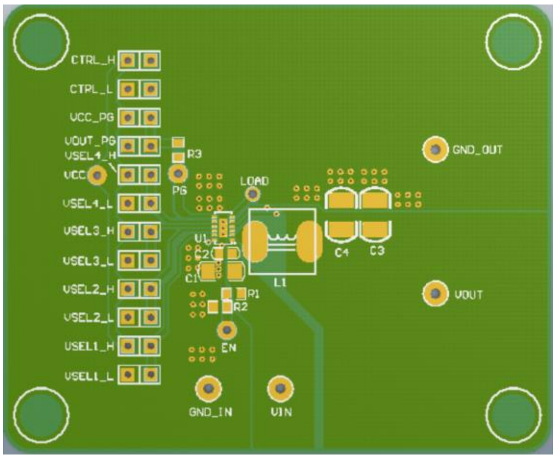


Figure 12. PCB Layout Recommendation

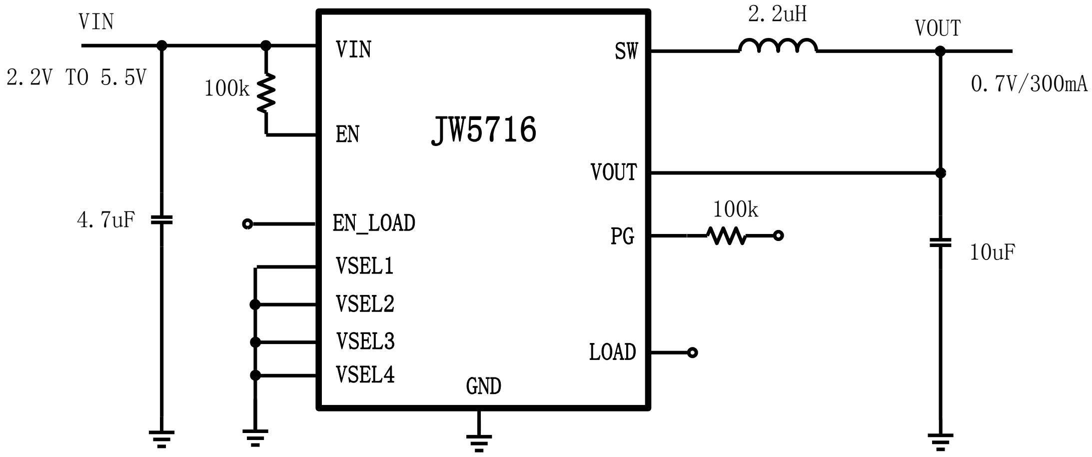
REFERENCE DESIGN

Reference:

V_{IN}: 2.3V ~ 5.5V

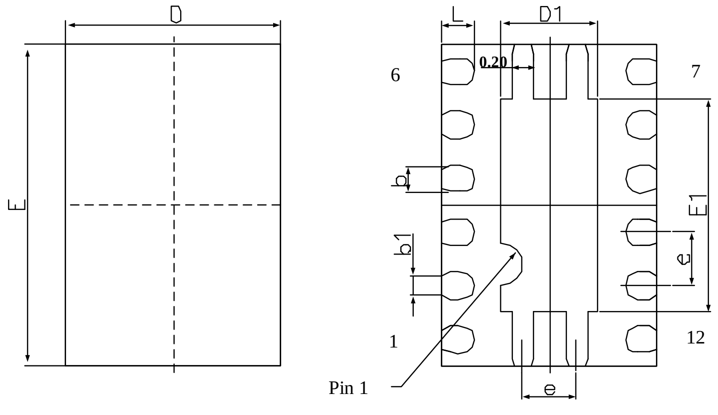
V_{OUT}: 0.7V

I_{OUT}: 0 ~ 300mA



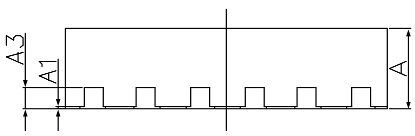
PACKAGE OUTLINE

DFN3X2-12 UNIT: mm



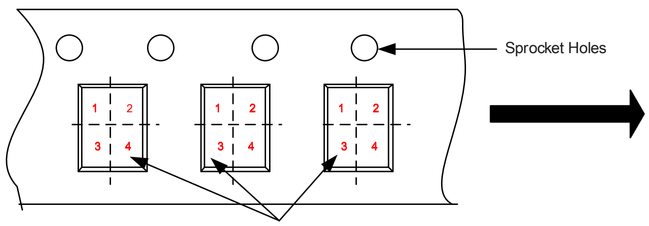
TOP VIEW BOTTOM VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	—	0.05
A3	0.20REF		
D	1.90	2.00	2.10
E	2.90	3.00	3.10
D1	0.80	0.90	1.00
E1	1.90	2.00	2.10
b	0.20	0.25	0.30
b1	0.18REF		
e	0.50BCS		
L	0.25	—	0.35



SIDE VIEW

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE



Package Type	Pin1 Quadrant
DFN3X2-12	1

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