JW5213H

3A, 6V, 1MHz, 50uA I_Q

Synchronous Step-Down Converter

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW®5213H is a current mode monolithic buck switching regulator. Operating with an input range of 2.5V-6V, the JW5213H delivers 3A of continuous output current with integrated P-Channel and N-Channel MOSFETs. The internal synchronous power switches provide high efficiency. At light loads, the regulator operate in low frequency to maintain high efficiency and low output ripples. Current mode control provides tight load transient response and cycle-by-cycle current limit.

The JW5213H guarantees robustness with hiccup output short-circuit protection, over-voltage protection, start-up current run-away protection, input under voltage lockout protection, hot-plug in protection, and thermal protection.

The JW5213H provides output power good indication.

The JW5213H is available in 8-pin DFN2X2-8 package, which provides a compact solution with minimal external components.

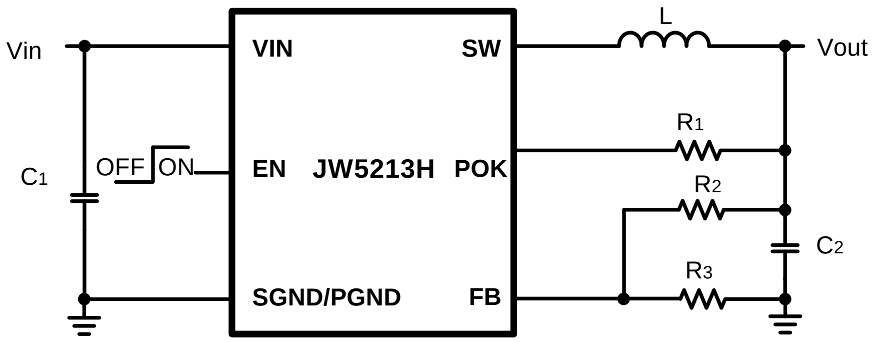
FEATURES

- 2.5V to 6V operating input range
- Up to 3A output current
- Up to 95% peak efficiency
- Internal soft-start
- 1MHz switching frequency
- Input under voltage lockout
- Short circuit protection
- Over voltage protection
- Thermal protection
- Hot-plug in protection
- Output POK indication
- RoHS compliant and halogen free
- Available in DFN2X2-8 package

APPLICATIONS

- 5V or 3.3V Point of Load Conversion
- Set Top Boxes
- Telecom/Networking Systems
- Storage Equipment
- GPU/DDR Power Supply

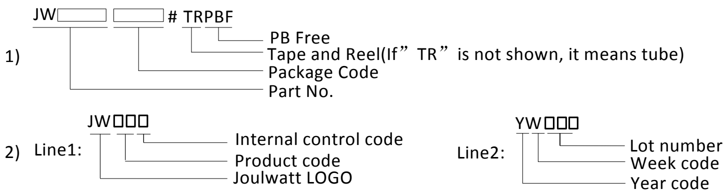
TYPICAL APPLICATION



ORDER INFORMATION

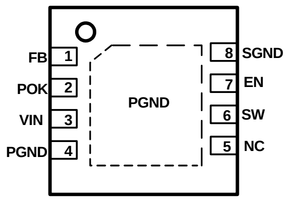
DEVICE[1]	PACKAGE	TOP MARKING[2]
JW5213HDFND#TRPBF	DFN2X2-8	JWFV□ YW□□□

Notes:



PIN CONFIGURATION

TOP VIEW



DFN2x2-8

ABSOLUTE MAXIMUM RATING[1)]

EN, FB, POK Pins..-0.3V to 7.0 V
Vin, SW Pins..-0.3V(-1.7V for 20ns) to 7.0V(8.0V for 10ns)
Junction Temperature.[2)] 150ºC
Lead Temperature.. 260ºC
Storage Temperature.. -65ºC to +150ºC
ESD Susceptibility (Human Body Model) 2kV

RECOMMENDED OPERATING CONDITIONS[3)]

Input Voltage VIN..2.5V to 6V
Output Voltage Vout..0.6V to VIN
Operating Junction Temperature..-40ºC to 125ºC

THERMAL PERFORMANCE[4)] θ_{JA} θ_{Jc}

DFN2x2-8..120…8.2ºC/W

Note:

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDE OPERATING CONDITIONS.

2) The JW5213H includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The device is not guaranteed to function outside of its operating conditions.

4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

VIN=5V, T_A=25℃, unless otherwise stated.						
Item	**Symbol**	**Condition**	**Min.**	**Typ.**	**Max.**	**Units**
V_{IN} Under Voltage Lockout Threshold	V_{IN_UVLO}	V_{IN} rising	2.25	2.4	2.55	V
V_{IN} Under Voltage Lockout Hysteresis	$V_{IN\_UVLO\_HYST}$			220		mV
V_{IN} Over Voltage Protection Threshold	V_{IN_OVP}	V_{IN} rising	6.5	6.85	7.2	V
V_{IN} Over Voltage Protection Hysteresis	$V_{IN\_OVP\_HYST}$			350		mV
Shutdown Current	I_{SHDN}	V_{EN}=0V		0.1	1	μA
Quiescent Current	I_Q	V_{EN}=2V, V_{FB}=V_{REF}*105%		50	80	μA
Regulated Feedback Voltage	V_{FB}	2.5V<V_{IN}<6V	0.588	0.6	0.612	V
PFET On Resistance	R_{DSON_P}	V_{IN}=3.6V, I_{SW}=200mA		110		mΩ
NFET On Resistance	R_{DSON_N}	V_{IN}=3.6V, I_{SW}=-200mA		90		mΩ
PFET Leakage Current	I_{LEAK_P}	V_{IN}=5.5V, V_{SW}=0V			1	uA
NFET Leakage Current	I_{LEAK_N}	V_{IN}=5.5V, V_{SW}=5.5V			1	uA
PFET Current Limit	I_{LIM_TOP}	Duty Cycle=100%	3.5	4.8		A
Switching Frequency	F_{SW}	I_{OUT}=1A	0.8	1	1.2	MHz
Minimum On Time[5)]	T_{ON_MIN}			80		ns
Maximum Duty Cycle	D_{MAX}			100		%
EN Rising Threshold	V_{EN_H}	V_{EN} rising, FB=0.4V			1	V
EN Falling Threshold	V_{EN_L}	V_{EN} falling, FB=0.4V	0.4			V
Short Circuit Protection Threshold[5)]	V_{SCP}			240		mV
POK Low Threshold	V_{POKL}	V_{FB} falling	510	540	570	mV
POK High Threshold	V_{POKH}	V_{FB} rising	690	720	750	mV
Over-voltage Protection Threshold	V_{OVP}	V_{FB} rising	690	720	750	mV
Over-voltage Deglitch Time	T_{OVP}			30		us
SW Discharge Resistance	R_{DISC}			50		Ω
Thermal Shutdown Threshold[5)]	T_{SHDN}			150		ºC
Temperature Hysteresis[5)]	T_{HYS}			15		ºC

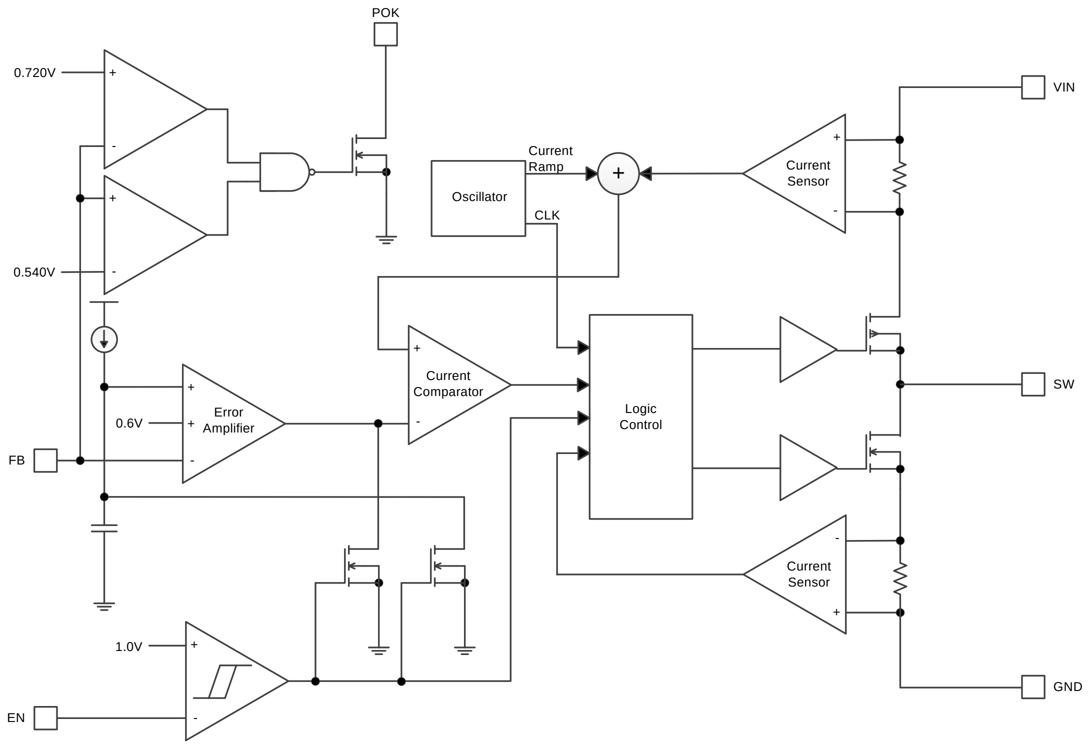
Note：

5) Guaranteed by design.

PIN DESCRIPTION

Pin	Name	Description
1	FB	Output feedback pin. FB senses the output voltage and is regulated by the control loop to 0.6V. Connect a resistive divider at FB.
2	POK	Open drain output. Connect a 10KΩ resistor from POK to output. POK is high when V_{FB} is within >90% and <120% of V_{REF}.
3	VIN	Input voltage pin. VIN supplies power to the IC. Connect a 2.5V to 6V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
4	PGND	Power ground pin.
5	NC	No connection.
6	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
7	EN	Drive EN pin high to turn on the regulator and low to turn off the regulator.
8	SGND	Signal ground pin.
Exposed Pad	PGND	Power ground pin.

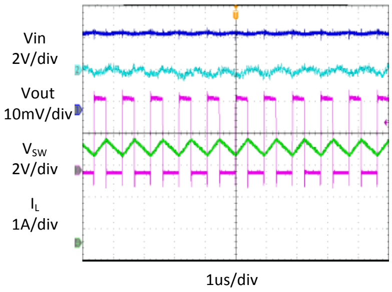
BLOCK DIAGRAM



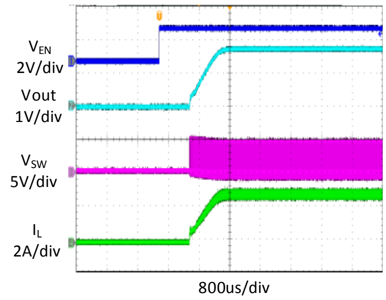
TYPICAL PERFORMANCE CHARACTERISTICS

Vin = 5V, Vout = 1.8V, L = 2.2μH, Cout = 44μF, TA = +25°C, unless otherwise noted

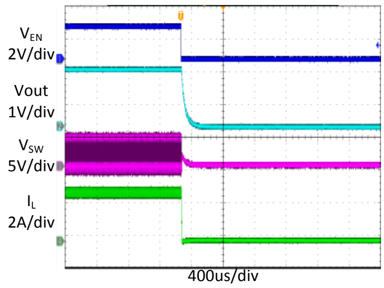
Steady State Test
VIN=5V, Vout=1.8V
Iout=3A



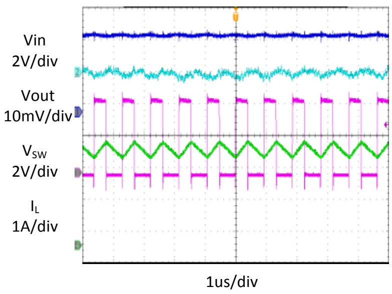
Startup through Enable
VIN=5V, Vout=1.8V
Iout=3A(Resistive load)



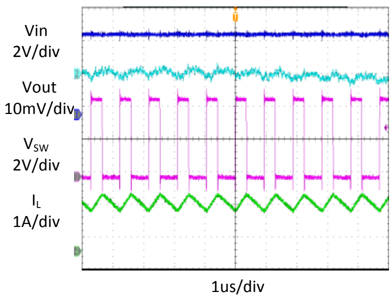
Shutdown through Enable
VIN=5V, Vout=1.8V
Iout=3A(Resistive load)



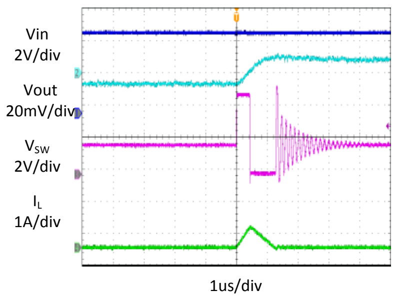
Heavy Load Operation
3A LOAD



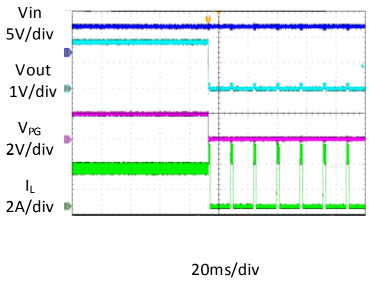
Medium Load Operation
1.5A LOAD



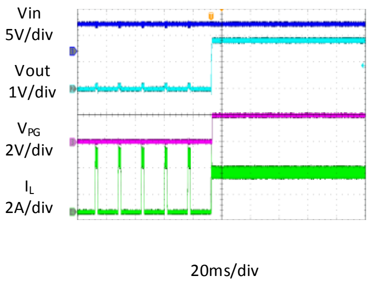
Light Load Operation
0 A LOAD



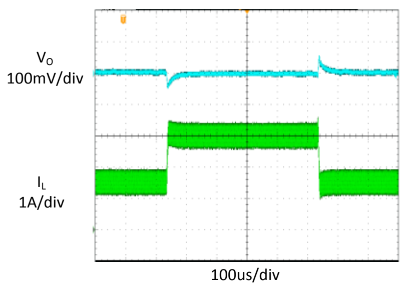
Short Circuit Protection
VIN=5V, Vout=1.8V
Iout=3A- Short



Short Circuit Protection
VIN=5V, Vout=1.8V
Iout= Short-3A



Load Transient
1.5A LOAD → 3A LOAD
→1.5A LOAD

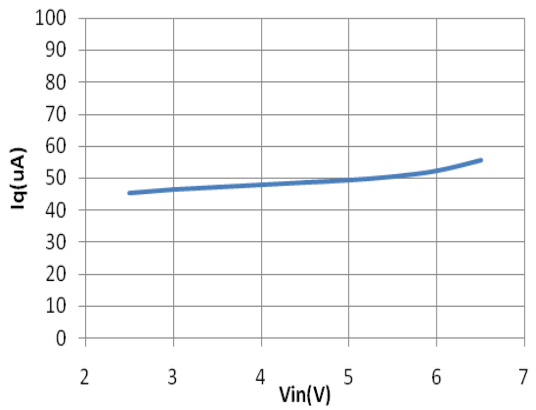


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Vin = 5V, Vout = 1.8V, L = 2.2μH, Cout = 44μF, TA = +25°C, unless otherwise noted

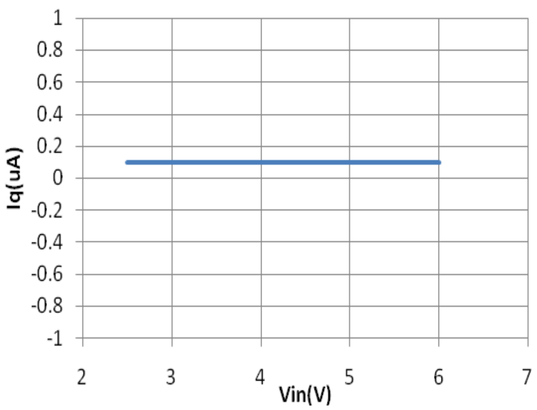
Quiescent Current Vs. Input Voltage

VIN=3V ~ 6.5V, VEN=3V, VFB=0.8V

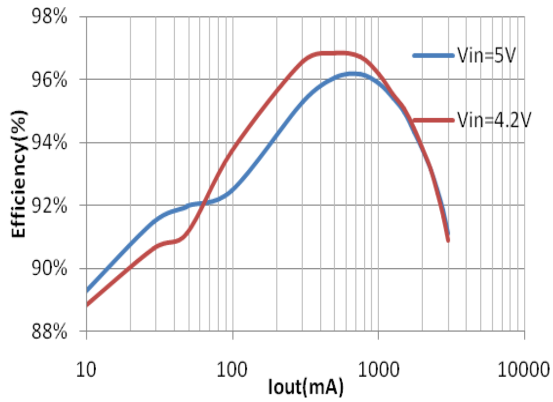


Shutdown Current Vs. Input Voltage

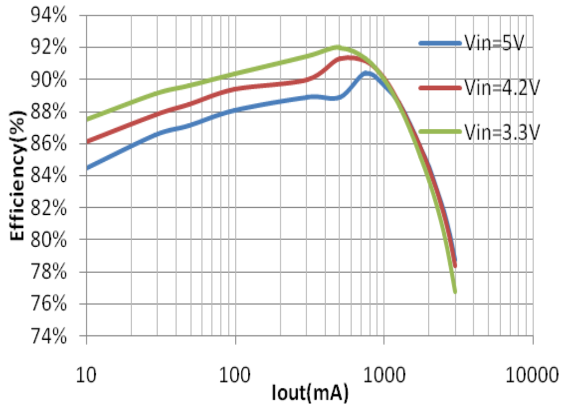
VIN=3V ~ 6.5V, VEN=0V, VFB=0.3V



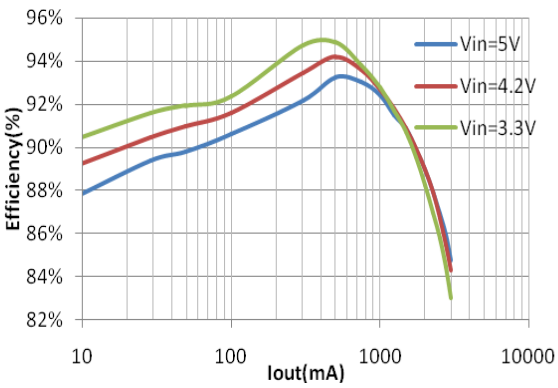
Efficiency @ Vout=3.3V



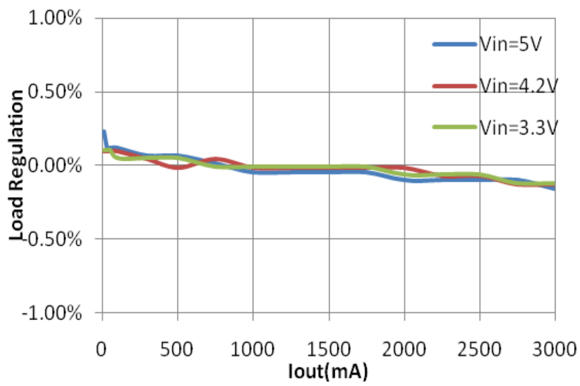
Efficiency @ Vout=1.2V



Efficiency @ Vout=1.8V



Load regulation @ Vout=1.8V



FUNCTIONAL DESCRIPTION

The JW5213H is a synchronous, current-mode, step-down regulator. It regulates input voltages from 2.5V~6V down to an output voltage as low as 0.6V, and is capable of supplying up to 3A of load current.

Current-Mode Control

The JW5213H utilizes current-mode control to regulate the output voltage. The output voltage is measured at the FB pin through a resistive voltage divider and the error is amplified by the internal transconductance error amplifier.
Output of the internal error amplifier is compared with the switch current measured internally to control the output current limit.

PFM Mode

The JW5213H operates in PFM mode at light load. In PFM mode, switch frequency is continuously controlled in proportion to the load current, i.e. switch frequency decreases when load current drops to boost power efficiency at light load by reducing switch-loss, while switch frequency increases when load current rises, minimizing output voltage ripple.

Shut-Down Mode

The JW5213H operates in shut-down mode when voltage at EN pin is driven below 0.4V. In shut-down mode, the entire regulator is off and the supply current consumed by the JW5213H drops below 1uA.

Power Switches

P-channel and N-channel MOSFET switches are integrated on the JW5213H to down convert the input voltage to the regulated output voltage.

Hot-Plug In Protection

If the Vin voltage exceeds 6.85V, IC will turn off power switch, entering over-voltage protection. It will remain in this state until Vin voltage is less than 6V.

Output Current Run-Away Protection

At start-up, due to the high voltage at input and low voltage at output, current inertia of the output inductance can be easily built up, resulting in a large start-up output current. A valley current limit is designed in the JW5213H so that only when output current drops below the valley current limit can the bottom power switch be turned off. By such control mechanism, the output current at start-up is well controlled.

Short Circuit Protection

When output is shorted to ground, the switching frequency is reduced to prevent the inductor current from increasing beyond PFET current limit. If short circuit condition holds for more than 1024 cycles, both PFET and NFET are forced off and can be enabled again after 12ms. This procedure is repeated as long as short circuit condition is not removed.

Over voltage protection

IC will shut down and enter overvoltage protection when output voltage is higher than 120% of regulation level for more than 20us. Output voltage will discharge by internal resister. Overvoltage protection will be removed when output voltage is lower than 120% of regulation level.

Thermal Protection

When the temperature of the JW5213H rises above 150°C, it is forced into thermal shut-down. Only when core temperature drops below 135°C can the regulator becomes active again.

APPLICATION INFORMATION

Output Voltage Set

The output voltage is determined by the resistor divider connected at the FB pin, and the voltage ratio is:

$$V_{FB} = V_{OUT} \cdot \frac{R_3}{R_2 + R_3}$$

where V_{FB} is the feedback voltage and V_{OUT} is the output voltage.

Choose R_3 around 10KΩ, and then R_2 can be calculated by:

$$R_2 = R_3 \cdot \left(\frac{V_{OUT}}{0.6V} - 1\right)$$

The following table lists the recommended values.

VOUT(V)	R2(KΩ)	R3(KΩ)
1.2	10	10
1.5	15	10
1.8	20	10
3.3	49.9	11

Input Capacitor

The input capacitor is used to supply the AC input current to the step-down converter and maintaining the DC input voltage. The ripple current through the input capacitor can be calculated by:

$$I_{C1} = I_{LOAD} \cdot \sqrt{\frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

where I_{LOAD} is the load current, V_{OUT} is the output voltage, V_{IN} is the input voltage.

Thus the input capacitor can be calculated by the following equation when the input ripple voltage is determined.

$$C_1 = \frac{I_{LOAD}}{f_S \cdot \Delta V_{IN}} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where C_1 is the input capacitance value, f_S is the switching frequency, $\triangle V_{IN}$ is the input ripple voltage.

The input capacitor can be electrolytic, tantalum or ceramic. To minimizing the potential noise, a small X5R or X7R ceramic capacitor, i.e. 0.1uF, should be placed as close to the IC as possible when using electrolytic capacitors.

A 22uF/0805/10V ceramic capacitor is recommended in typical application.

Output Capacitor

The output capacitor is required to maintain the DC output voltage, and the capacitance value determines the output ripple voltage. The output voltage ripple can be calculated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \cdot \left(R_{ESR} + \frac{1}{8 \cdot f_S \cdot C_2}\right)$$

where C_2 is the output capacitance value and R_{ESR} is the equivalent series resistance value of the output capacitor.

The output capacitor can be low ESR electrolytic, tantalum or ceramic, which lower ESR capacitors get lower output ripple voltage.

The output capacitors also affect the system stability and transient response, and two 22uF/0805/6.3V ceramic capacitors are recommended in typical application.

Inductor

The inductor is used to supply constant current to the output load, and the value determines the ripple current which affect the efficiency and the output voltage ripple. The ripple current is typically allowed to be 30% of the maximum switch current limit, thus the inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_S \cdot \Delta I_L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_S is the switching frequency, and $\triangle I_L$ is the peak-to-peak inductor ripple current.

PCB Layout Note

For minimum noise problem and best operating performance, the PCB is preferred to following the guidelines as reference.

1. Place the input decoupling capacitor as close to JW5213H (VIN pin and PGND) as possible to eliminate noise at the input pin. The loop area formed by input capacitor and GND must be minimized.
2. Put the feedback trace as far away from the inductor and noisy power traces as possible.
3. The ground plane on the PCB should be as large as possible for better heat dissipation.

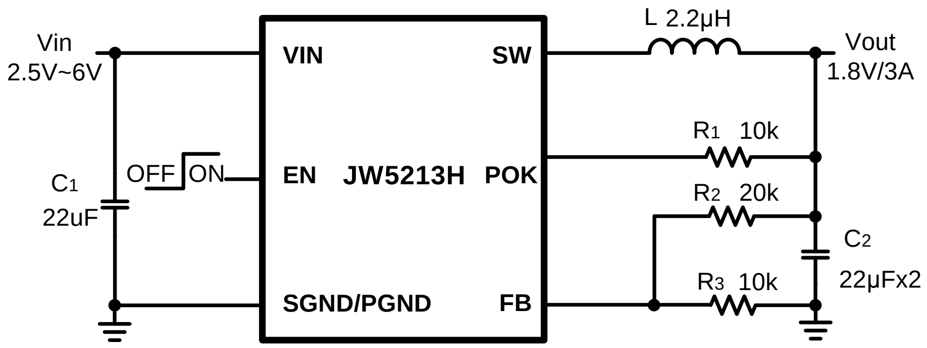
REFERENCE DESIGN

Reference 1:

V_{IN}: 2.5V ~ 6V

V_{OUT}: 1.8V

I_{OUT}: 0~3A

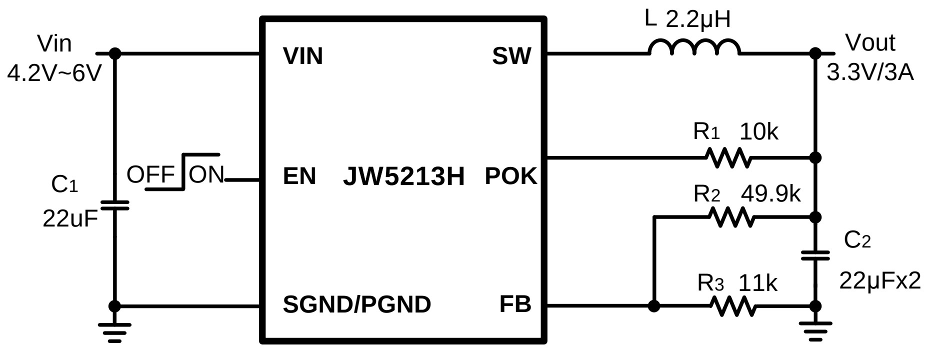


Reference 2:

V_{IN}: 4.2V ~ 6 V

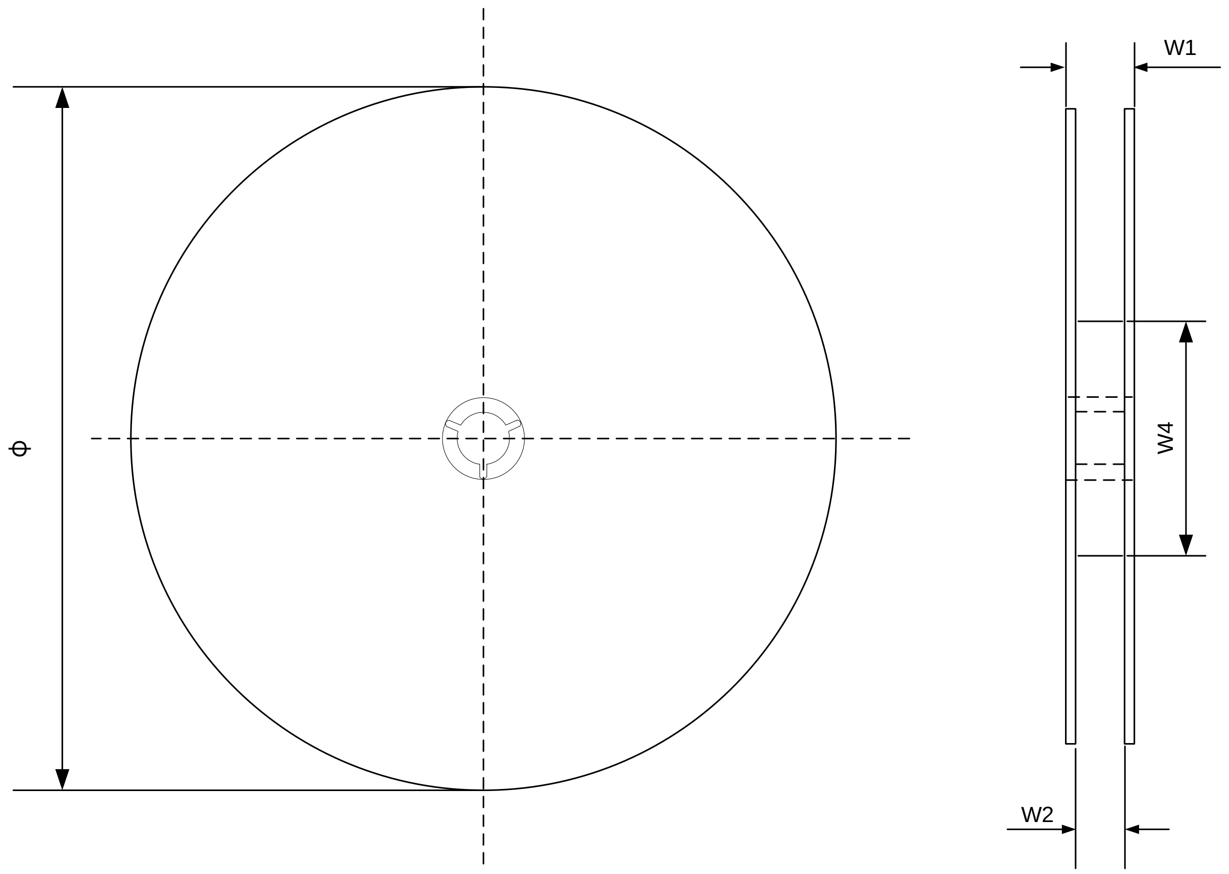
V_{OUT}: 3.3V

I_{OUT}: 0~3A



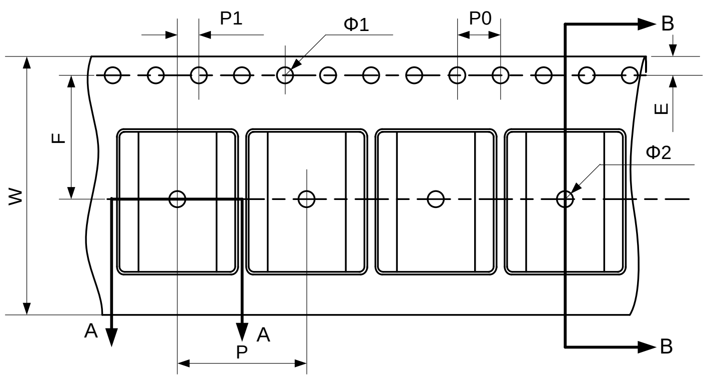
TAPE AND REEL INFORMATION

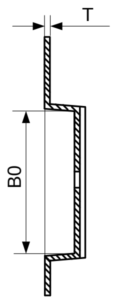
Reel UNIT: mm



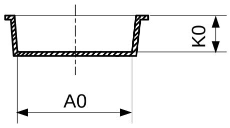
Package	Diameter Φ	Thickness W1	Width W2	W4
DFN2x2-8	178±2	12.30±2	9.5±2	60±2

Carrier Tape UNIT: mm





SECTION B-B

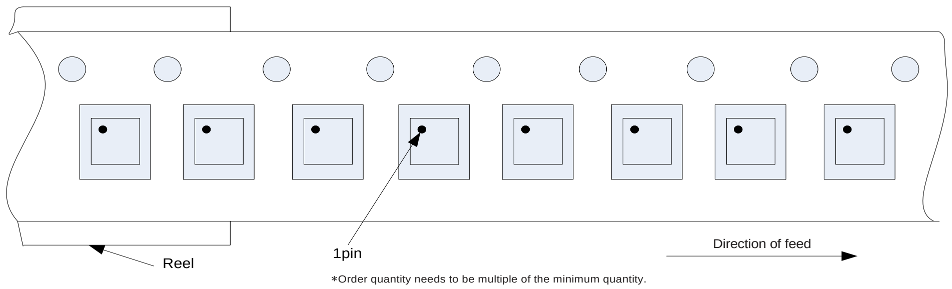


SECTION A-A

Note :

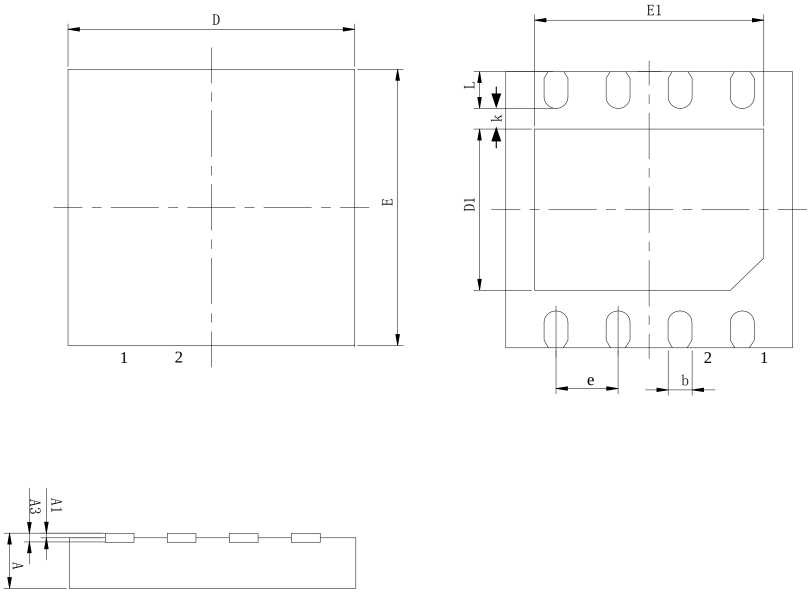
1) The carrier type is black, and colorless transparent.
2) Carrier camber is within 1mm in 100mm.
3) 10 pocket hole pitch cumulative tolerance:±0.20.
4) All dimensions are in mm.

Package	P0	P1	P	A0	B0	W	T0	K0	Φ1	Φ2	E	F
DFN 2x2-8	4.00±0.10	2.00±0.10	4.00±0.10	2.30±0.20	2.30±0.20	8.00±0.30	0.25±0.20	1.00±0.35	1.50min	1.00min	1.75±0.10	3.50±0.10



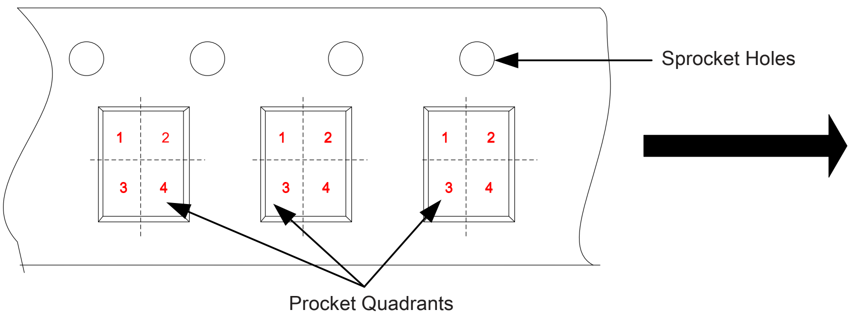
PACKAGE OUTLINE

DFN2X2-8 UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	—	0.05
A3	0.20REF		
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D1	0.50	0.60	0.70
E1	1.10	1.20	1.30
k	0.35REF		
b	0.20	0.25	0.30
e	0.50BCS		
L	0.27	—	0.43

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE



Package Type	Pin1 Quadrant
DFN2x2-8	1

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