16V/16A Synchronous Step-Down Converter

ESCRIPTION

The JWH5086A is a monolithic buck switching regulator based on I2 architecture for fast transient response. Operating with an input range of 2.7V~16V, JWH5086A delivers 16A of continuous output current with two integrated N-Channel MOSFETs. The internal synchronous power switches provide high efficiency without the use of an external Schottky diode. The operation frequency is set easily to 700 kHz, 800 kHz, or 1000 kHz with the MODE configuration, allowing the JWH5086A frequency to remain constant regardless of the input and output voltages.

JWH5086A guarantees robustness with output short protection, over-voltage protection, thermal protection and under voltage protection.

JWH5086A is available in QFN3×4-21 package, which provides a compact solution with minimal external components.

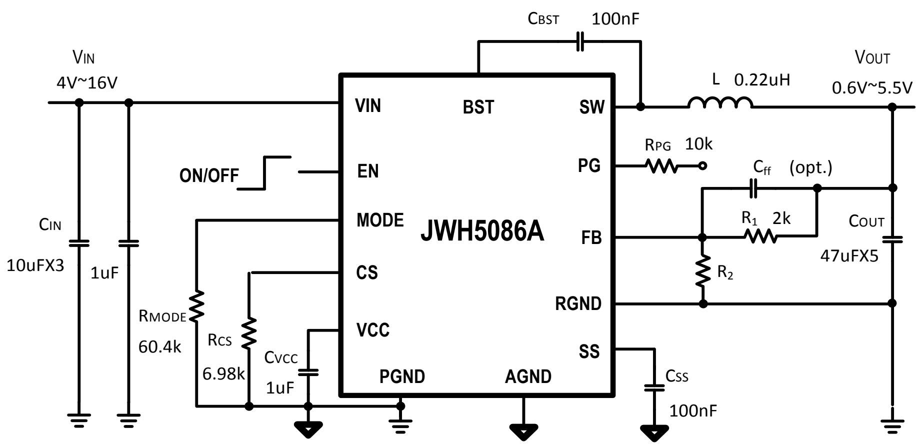
FEATURES

- 2.7V to 16V Operating Input Range with External 3.3V VCC Bias
- 4V to 16V Operating Input Range with Internal Bias or External 3.3V VCC Bias
- 16A output current
- Differential Output Voltage Remote Sense
- Programmable Accurate Current Limit Level
- ±0.5% Reference Voltage over 0℃ to +70℃ Junction Temperature Range
- FCCM Operation Mode
- Power Good Indicator
- Programmable Soft-Start Time
- Selectable Switching Frequency from 700kHz, 800kHz, and 1000kHz
- Output Discharge Function
- Non-Latch OCP, UVP, OVP, UVLO
- Thermal Protection
- Available in QFN3X4-21 Package

APPLICATIONS

- Telecom and Networking Systems
- Server, Cloud-Computing, Storage
- Base Stations
- General Purpose Point-of-Load

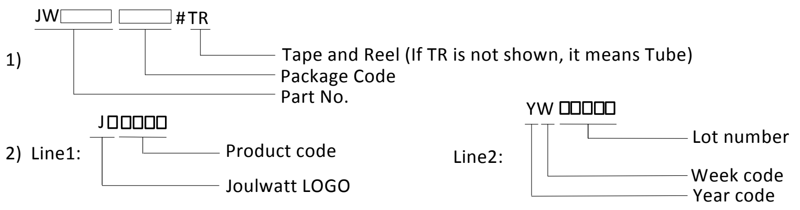
TYPICAL APPLICATION



ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]	ENVIRONMENTAL[3)]
JWH5086AQFNAG#TR	QFN3X4-21	JH5086A YW□□□□□	Green

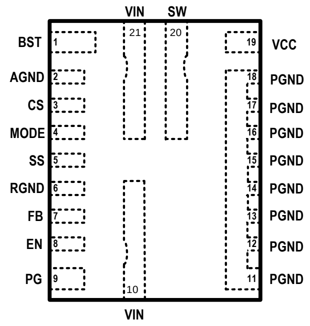
Notes:



3) All JoulWatt products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

PIN CONFIGURATION

TOP VIEW



ABSOLUTE MAXIMUM RATING[1)]

VIN Pin……... -0.3V to 18V
SW Pin.. -0.3V (-5V for 25ns) to 18V (25V for 25ns)
VIN-SW...-0.3V (-5V for 25ns) to 18.3V (25V for 25ns)
BST-SW .... -0.3V to 4V (5V for 25ns)
VCC Pin .... -0.3V to 4V
All other Pins .... -0.3V to 4V
Junction Temperature [2)] 150ºC
Lead Temperature 260ºC
Storage Temperature………………………………………………………………………...-65 ºC to +150 ºC
ESD Susceptibility (Human Body Model) ....±2kV
Charged device model (CDM), per JEDEC specification JESD22- V C101.................................. ±500V

RECOMMENDED OPERATING CONDITIONS[3)]

Input Voltage V_{IN} .... 4V to 16V
Output Voltage V_{OUT} .... 0.6V to 5.5V
External VCC Bias V_{CC_EXT} .... Up to 3.6V
Maximum Internal VCC Output Current I_{VCC_MAX} 150mA
Maximum Output Current I_{OUT_MAX} 16A
Maximum Output Current Limit I_{OC_MAX} 20A
Maximum Peak Inductor Current Limit I_{L_Peak} 30A
Operation Junction Temperature T_j.. .... -40°C to 125°C

THERMAL PERFORMANCE[4)]

	θ_{JB} [5)]	θ_{Jc_TOP} [5)]
QFN3X4-21	8	18°C/W

Note:

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.
2) The JWH5086A includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.
5) θ_{JB} Thermal resistance from junction to board around PGND pin soldering point.
   θ_{Jc_TOP} Thermal resistance from junction to top of package.

ELECTRICAL CHARACTERISTICS

VIN=12V, T_J=-40℃~125℃，Unless otherwise stated.

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
V_{IN} Under Voltage Lock-out Threshold	V_{IN_HTH}	V_{IN} rising, V_{CC}=3.3V	2.1	2.4	2.7	V
	V_{IN_LTH}	V_{IN} falling, V_{CC}=3.3V	1.55	1.85	2.15	V
Shutdown Current	I_{SD}	V_{EN} =0		0.5	5	μA
Supply Current	I_Q	V_{EN}=2V, V_{FB}=0.7V		550	800	μA
Enable Input Rising Threshold	V_{EN_HTH}		1.17	1.22	1.27	V
Enable Hysteresis	$V_{EN\_TH\_HYS}$			200		mV
Enable Input Current	I_{EN}	V_{EN}=2V		0		μA
Feedback Voltage	V_{REF}	T_J=-40℃ to 125℃	594	600	606	mV
		T_J= 0℃ to 70℃	597	600	603	mV
Feedback Current	I_{FB}	V_{FB}=0.6V		10	100	nA
Top Switch Resistance	$R_{DS(ON)T}$			8.9	13.8	mΩ
Bottom Switch Resistance	$R_{DS(ON)B}$			2.6	4.8	mΩ
Top Switch Leakage Current	I_{LEAK_TOP}	V_{IN}=16V, V_{SW}=0V			10	μA
Bottom Switch Leakage Current	I_{LEAK_BOT}	V_{IN}=16V, V_{SW}=16V			10	μA
Current Limit Threshold	V_{LIM}		1.15	1.2	1.25	V
ICS to IOUT Ratio	I_{CS}/I_{OUT}	R_{CS} =6K	8	9	11	μA/A
Bottom Switch Negative Current Limit	I_{LIM_NEG}		-21	-16	-12	A
Minimum On Time[6)]	T_{ON_MIN}				50	ns
Minimum Off Time[6)]	T_{OFF_MIN}			100	180	ns
Switching Frequency	F_{SW}	MODE=GND	560	660	760	kHz
		MODE=30.1K	640	750	860	kHz
		MODE=60.4K	860	970	1080	kHz
Discharge FET Ron	R_{DIS}			110	200	Ω
Soft-Start Charge Current	I_{SS_CHAR}	V_{SS}=0V		42		μA
Soft-Start Pull Down Current	$I_{SS\_DISCHAR}$	V_{SS}=1V	0.4	0.55	0.7	mA
Soft-Start Time[6)]	T_{SS}	C_{SS}=1nF	0.5	1	1.5	ms
VCC Under-voltage Lockout Threshold	V_{CC_HTH}	V_{CC} rising	2.65	2.8	2.95	V
	V_{CC_LTH}	V_{CC} falling	2.35	2.5	2.65	V
VCC Regulator	V_{CC}		3.1	3.2	3.35	V
VCC Load Regulation		I_{CC}=100mA		0.5		%
Power Good High Threshold	$PG_{\_HTH}$	V_{FB} from low to high	89.5%	92.5%	95.5%	V_{REF}
		V_{FB} from high to low	102%	105%	108%	V_{REF}
Power Good Low Threshold	$PG_{\_LTH}$	V_{FB} from low to high	113%	117%	121%	V_{REF}
		V_{FB} from high to low	77%	80%	83%	V_{REF}

VIN=12V, T_J=-40℃~125℃, Unless otherwise stated.						
Item	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Power Good Delay Time	$PG_{\_DLY}$	V_{PG} from low to high	0.7	1.1	1.5	ms
Power Good Sink Current	I_{PG}	V_{PG} =0.5V	3			mA
Power Good Leakage Current	I_{LEAK_PG}	V_{PG}=3.3V		3.5	5	μA
Power Good Low-level Output Voltage	V_{OL_100}	V_{IN}=0V, Pull PG up to 3.3V through a 100kΩ resistor		520	800	mV
	V_{OL_10}	V_{IN}=0V, Pull PG up to 3.3V through a 10kΩ resistor		620	900	mV
Output Over-voltage Threshold		V_{FB} Rising	113%	117%	121%	V_{REF}
Output Under-voltage Threshold		V_{FB} Falling	77%	80%	83%	V_{REF}
Output UVP Delay	T_{DLY_UVP}			1.7		μs
UVP/OCP Hiccup OFF Time	T_{HICCUP_OFF}			12		ms
Thermal Shutdown[6)]	T_{TSD}			160		°C
Thermal Shutdown Hysteresis[6)]	T_{TSD_HYST}			30		°C
Power On Delay Time	$T_{DLY\_POWERON}$			95		μs

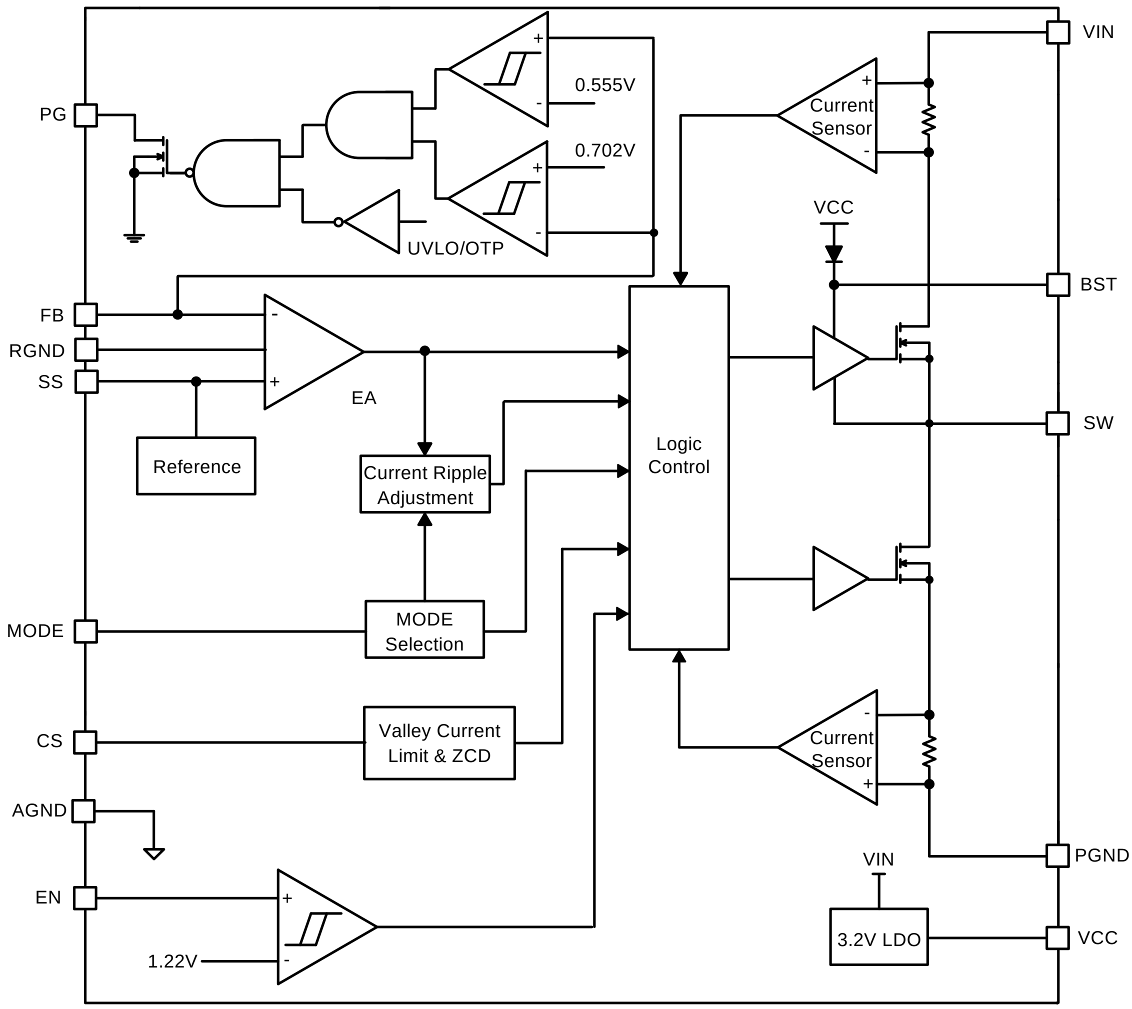
Note:

6) Guaranteed by design.

PIN DESCRIPTION

Pin	Name	Description
1	BST	Connect a 0.1uF capacitor between BST and SW pin to supply current for the top switch driver.
2	AGND	Analog ground pin. Select AGND as the control circuit reference point.
3	CS	Current limit. Connect a resistor to AGND to set the current limit trip point.
4	MODE	Frequency selection. Program MODE to select the operating switching frequency.
5	SS	Soft-start time setting pin. The soft-start time is determined by the capacitance between SS pin and AGND.
6	RGND	Differential remote sense negative input. Connect this pin directly to the negative side of the voltage sense point. Short to GND if remote sense is not used.
7	FB	Feedback (Differential remote sense positive input). An external resistor divider from the output to RGND (tapped to FB) sets the output voltage. It is recommended to place the resistor divider as close to FB as possible. Vias should be avoided on the FB traces.
8	EN	Enable control pin. Pull this pin high to turn on the regulator. Do not leave this pin floating.
9	PG	Power good monitor output. Open drain output when the output voltage is within 92.5% to 117% of internal reference voltage.
10, 21	VIN	Input voltage pin. VIN supplies power to the IC. Connect a 2.7V to 16V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
11-18	GND	Power ground pin
19	VCC	Internal 3.2V LDO Output. Power supply for internal analog circuits and driving circuit. Decouple this pin to ground with a minimum 1uF ceramic capacitor.
20	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.

BLOCK DIAGRAM



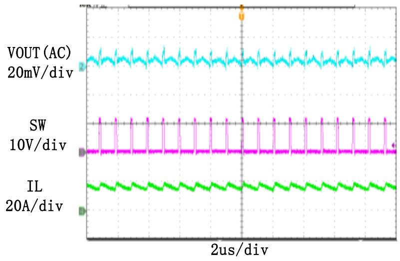
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1.2V, L = 0.22μH, C_{OUT} = 47μF×5, F_{SW} = 700kHz, T_A = +25°C, unless otherwise noted.

Steady State Test

V_{IN}=12V, V_{OUT}=1.2V

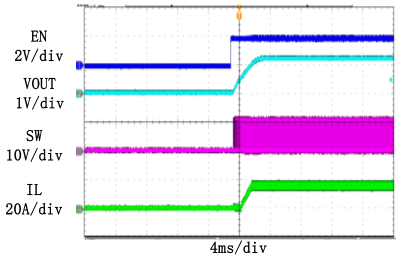
I_{OUT}=16A



Startup through Enable

V_{IN}=12V, V_{OUT}=1.2V

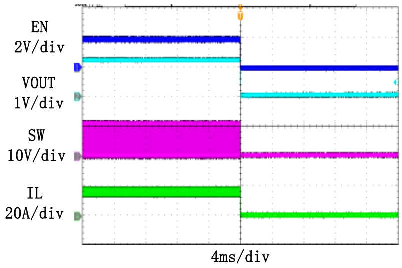
I_{OUT}=16A



Shutdown through Enable

V_{IN}=12V, V_{OUT}=1.2V

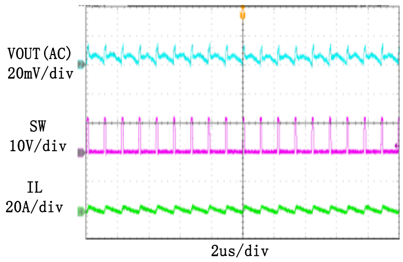
I_{OUT}=16A



Steady State Test

V_{IN}=12V, V_{OUT}=1.2V

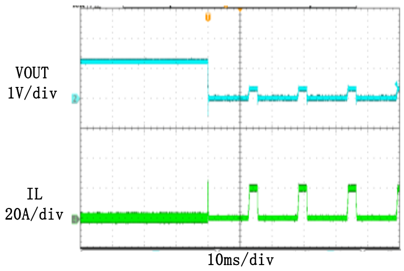
I_{OUT}=0A



Short Circuit Protection

V_{IN}=12V, V_{OUT}=1.2V

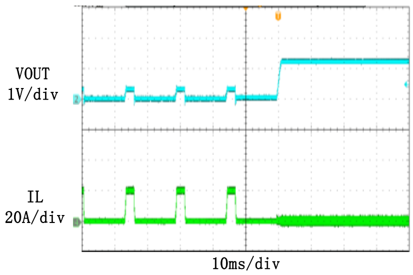
I_{OUT}=0A→Short



Short Circuit Recovery

V_{IN}=12V, V_{OUT}=1.2V

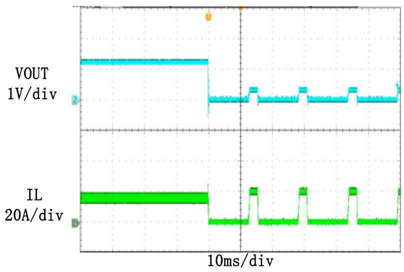
I_{OUT}=Short→0A



Short Circuit Protection

V_{IN}=12V, V_{OUT}=1.2V

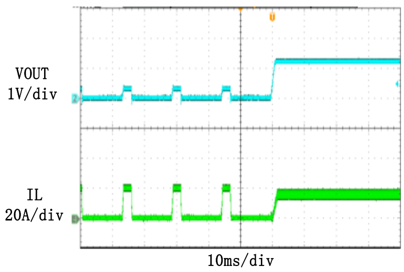
I_{OUT}=16A→Short



Short Circuit Recovery

V_{IN}=12V, V_{OUT}=1.2V

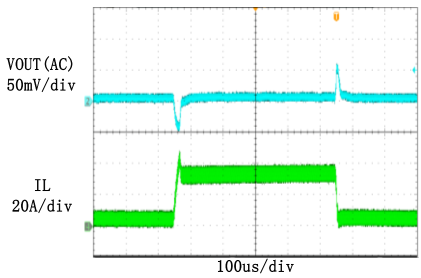
I_{OUT}=Short→16A



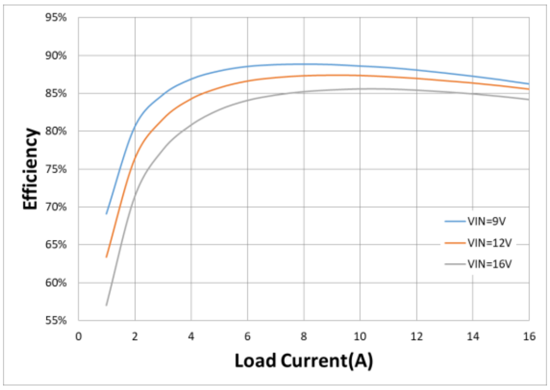
Load Transient

V_{IN}=12V, V_{OUT}=1.2V

I_{OUT}=1.6A~16A

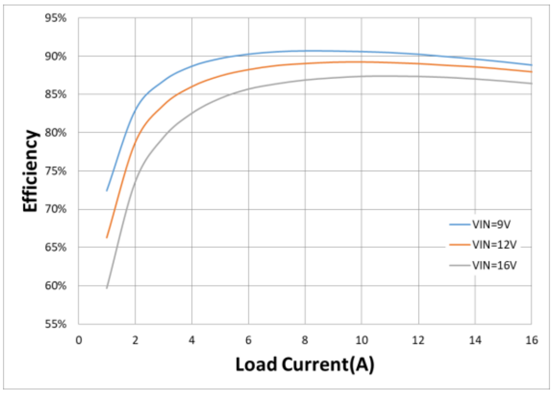


TYPICAL PERFORMANCE CHARACTERISTICS



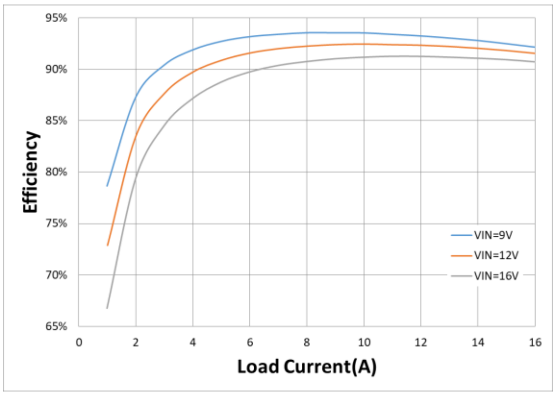
Efficiency vs. Load Current

(V_{OUT}=1.2V, L=0.22uH, F_{SW}=700kHz)



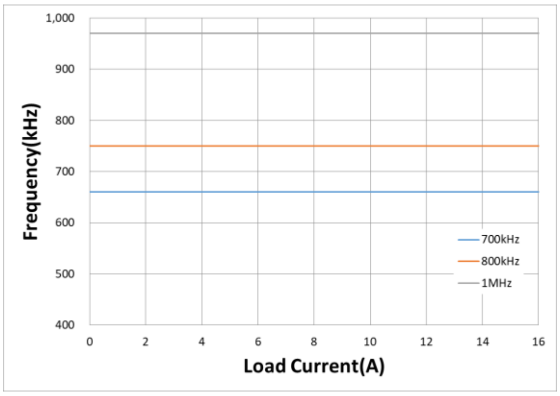
Efficiency vs. Load Current

(V_{OUT}=1.8V, L=0.22uH, F_{SW}=1MHz)



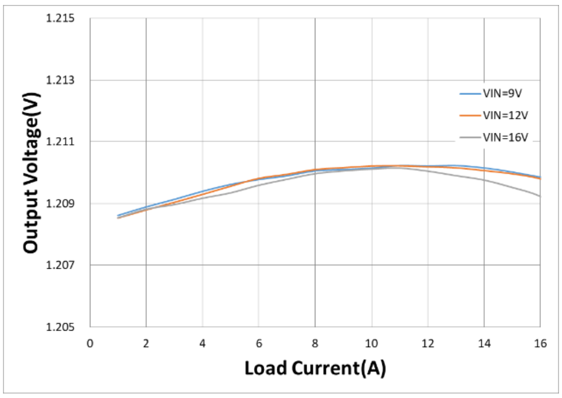
Efficiency vs. Load Current

(V_{OUT}=3.3V, L=0.22uH, F_{SW}=1MHz)



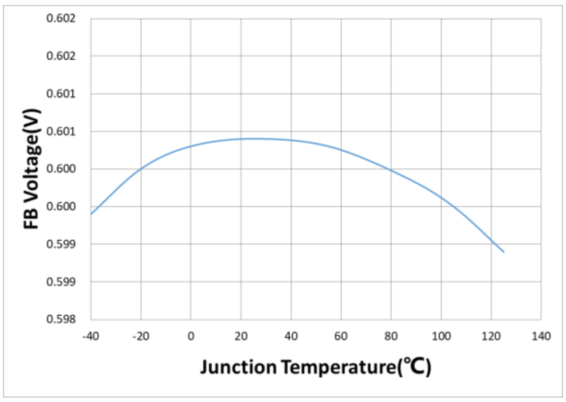
Frequency vs. Load Current

(V_{IN}=12V, V_{OUT}=1.8V, L=0.22μH)



Load Regulation

(V_{OUT}=1.2V, L=0.22uH, F_{SW}=700kHz)



FB Voltage Regulaion vs. Junction Temperature

FUNCTIONAL DESCRIPTION

JWH5086A is a synchronous step-down regulator based on I2 control architecture. It regulates input voltages from 2.7V to 16V down to as low as 0.6V output voltage, and is capable of supplying up to 16A of load current.

Power Switch

N-Channel MOSFET switches are integrated on the JWH5086A to down convert the input voltage to the regulated output voltage. Since the top MOSFET needs a gate voltage greater than the input voltage, a boost capacitor connected between BST and SW pins is required to drive the gate of the top switch. The boost capacitor is charged by the internal/external rail when SW is low.

Frequency Selection

JWH5086A operates in forced continuous conduction mode (FCCM), and the switching frequency is fairly constant; hence the output ripple keeps almost the same throughout the whole load range.

JWH5086A has three options for switching frequency selection. Selecting the switching frequency is done by choosing the resistance value of the resistor connected between MODE and AGND (See Table 1).

Table 1 --- Frequency selection

MODE	Switching Frequency[7]
GND	700kHz
30.1kΩ(±20%) to GND	800kHz
60.4kΩ(±20%) to GND	1000kHz

Note:

7) Refer to ELECTRICAL CHARACTERISTICS for more accurate switching frequency data.

Shut-Down Mode

The JWH5086A shuts down when voltage at EN pin is below 0.3V. The entire regulator is off and the supply current consumed by the JWH5086A drops below 5uA.

V_{IN} Under-Voltage Protection

In addition to the enable function, the JWH5086A provides an Under Voltage Lock-out (UVLO) function that monitors the input voltage. To prevent operation without fully-enhanced internal MOSFET switches, this function inhibits switching when input voltage drops below the UVLO-falling threshold. The IC resumes switching when input voltage exceeds the UVLO-rising threshold.

Enable and Adjustable UVLO Protection

The JWH5086A is enabled when the VIN pin voltage rises above 2.4V and the EN pin voltage exceeds the enable threshold of 1.22V. The JWH5086A is disabled when the VIN pin voltage falls below 1.85V or when the EN pin voltage is below 1.02V. Do not leave this pin floating.

If an application requires a higher V_{IN} under-voltage lockout (UVLO) threshold, use a resistive divider connected between VIN and ground with the central tap connected to EN to adjust the input voltage UVLO. (Shown in Figure 1). So that when V_{IN} rises to the pre-set value, V_{EN} rises above 1.22V to enable the device and when V_{IN} drops below the pre-set value, V_{EN} drops below 1.02V to trigger input under voltage lockout protection.

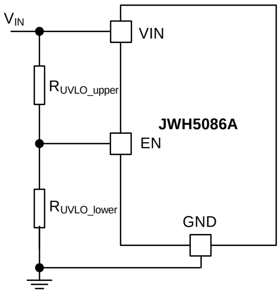


Figure. 1 Adjustable UVLO

The input voltage UVLO threshold (V_{UVLO}) and hysteresis (V_{UVLO_HYS}) can be calculated by the following equation.

$$V_{UVLO} := \frac{R_{UVLO\_upper} + R_{UVLO\_lower}}{R_{UVLO\_lower}} \cdot V_{EN\_TH}$$

$$V_{UVLO\_HYS} := \frac{R_{UVLO\_upper} + R_{UVLO\_lower}}{R_{UVLO\_lower}} \cdot V_{EN\_HYS}$$

where
V_{EN_TH} is enable shutdown threshold (1.22V typ.);
V_{EN_HYS} is enable shutdown hysteresis (200mV typ.).

Soft Start

Soft-start is designed in JWH5086A to prevent the converter output voltage from overshooting during startup and short-circuit recovery. An internal current source (I_{SS}) of 42uA is designed to charge the external soft-start capacitor (C_{SS}) and generates a soft-start (SS) voltage ramping up from 0V to 1.5V. When it is less than internal reference voltage ($V_{REF,}$ typ. 0.6V), SS voltage overrides V_{REF} and the error amplifier uses SS voltage as the reference. When SS exceeds V_{REF}, V_{REF} regains control.

The soft start time (10% to 90%) T_{SS} can be calculated by the following equation.

$$T_{SS}(ms) := \frac{C_{SS}(nF) \cdot V_{REF}(V) \cdot 0.8}{I_{SS}(\mu A)}$$

where C_{SS} is the soft-start capacitance connected between SS pin and AGND pin.

The JWH5086A has a configured external soft start time and a constant internal soft start time, it will follow the slower one between them. Therefore, the minimum soft start time is about 1ms even a smaller capacitor is used. The soft start will not be ready until both the internal and external SS voltage exceeds 0.85V.

At power up, the soft start pin is discharged before MOSFETs switching to ensure a proper power up. Also, during normal operation, the JWH5086A will stop switching and the soft-start pin will be discharged, when the V_{IN} UVLO is exceeded, EN pin pulled below 1.02V, or a thermal shutdown event occurs.

Current Sense and Over-Current Protection (OCP)

The JWH5086A features an on-die current sense and a programmable positive current limit threshold.

The cycle-by-cycle current limit is activated when the JWH5086A is enabled. The SW valley current limit is proportional to I_{CS} current, which is set by a resistor (R_{CS}) from CS to AGND.

The following equation calculates the current limit threshold setting from R_{CS}:

$$R_{CS}(\Omega) := \frac{V_{OCP}}{G_{CS} \cdot \left[I_{LIM} - \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{V_{IN}} \cdot \frac{1}{2 \cdot L \cdot f_{SW}} \right]}$$

where

V_{OCP}=1.2V,
G_{CS} = 9 μA/A, and
I_{LIM} = the desired output current limit.

The OCP HICCUP is active 3ms after the JWH5086A is enabled, Once OCP HICCUP is active, if the JWH5086A detects over-current condition for consecutive 31 cycles, or if the FB drops below under-voltage protection (UVP) threshold, it enters HICCUP mode. In HICCUP mode, the JWH5086A latches off the high side MOSFET immediately, and latches off low side

MOSFET after ZCD is detected. Meanwhile, the SS capacitor is also discharged. After about 12ms, the JWH5086A will try to soft start automatically. If the over-current condition still holds after 3ms of running, the JWH5086A repeats this operation cycle until the over-current condition disappears, and the output voltage rises smoothly back to the regulation level.

Negative Inductor Current limit

When the low side MOSFET detects a -16A current, the part turns off the low side MOSFET to limit the negative current.

Pre-Bias Start-Up

The JWH5086A has been designed for a monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the IC disables switching for both the high-side and low-side MOSFETs until the voltage on the SS capacitor exceeds the sensed output voltage at FB. Before SS voltage reaches pre-biased FB level, if the BST voltage (from BST to SW) is lower than 1.8V, the low-side MOSFET is turned on to allow the BST voltage to be charged through VCC. The low-side MOSFET is turned on for very narrow pulses, so the drop in pre-biased level is negligible.

Output Voltage Discharge

When the JWH5086A is disabled through EN, it enables the output voltage discharge mode. This causes both the high side MOSFET and the low side MOSFET to latch off. A discharge FET connected between SW and PGND is turned on to discharge the output voltage. The typical switch on resistance of this FET is about 110Ω. Once the FB voltage drops below 10%* V_{REF}, the discharge FET is turned off.

Output Over-voltage Protection

The JWH5086A monitors the output voltage by connecting FB to the tap of the output voltage feedback resistor divider to detect an overvoltage condition. This provides auto-recovery OVP mode.

If the FB voltage is between 105% and 117% of REF voltage, the low side MOSFET remains on until it hits the low-side negative current limit (NOCP). Once it hits NOCP, the low side MOSFET is turned off and the high side MOSFET is turned on until the negative current reaches to zero. The JWH5086A keeps this operation to try to bring down the output voltage.

If the FB voltage furtherly exceeds 117% of the REF voltage, it enters OVP mode. The high side MOSFET is turned off and the low side MOSFET remains on until it hits NOCP. Once it hits NOCP, the power MOSFETs stop switching. The power MOSFETs would not restart switching until the FB voltage drops below 105% of REF voltage. PGOOD goes low until the FB voltage drops below 105% of REF voltage.

Power Good

The JWH5086A has power-good (PG) output. The PG pin is the open drain of a MOSFET. Connect to VCC or another voltage source through a resistor. After applying the input voltage, the power MOSFETs start switching, PG is pulled to GND before SS is ready. After the FB voltage reaches 92.5% of the REF voltage and soft start is ready, PG is pulled high after a 1.1ms delay.

When the FB voltage drops to 80% of the REF voltage, PG is pulled low within 1.7us deglitch time. When the FB voltage rises above 92.5% of the REF voltage, PG is pulled high again after a 1.1ms delay time.

When the FB voltage exceeds 117% of the REF voltage, PG is pulled low within 1.7us deglitch time. When the FB voltage drops to 105% of the REF voltage, PG is pulled high again with 1.1ms deglitch time.
Once EN UVLO or OTP is triggered, PG is pulled low within 1.7us deglitch time even FB voltage is

still in threshold range.

If the input supply fails to power the JWH5086A, PG is clamped low even though PG is tied to an external DC source through a pull-up resistor.

Thermal Protection

When the temperature of the JWH5086A rises above 160°C, it is forced into thermal shut-down and SS capacitor is discharged.

Only when core temperature drops below 130°C can the regulator become active again.

APPLICATION INFORMATION

Output Voltage Set

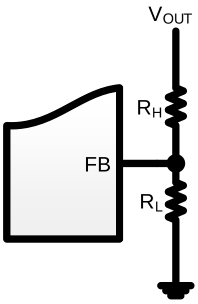
The output voltage is determined by the resistor divider connected at the FB pin, and the voltage ratio is:

$$V_{FB} = V_{OUT} * \frac{R_L}{R_H + R_L}$$

where V_{FB} is the feedback voltage and V_{OUT} is the output voltage.

To improve efficiency at very light load, using larger value resistors is preferred. However, using too high of resistance causes the circuit to be more susceptible to noise, and voltage errors from the V_{FB} input current will be more noticeable. If R_H is determined, such as 2kΩ, and then R_L can be calculated by:

$$R_L = \frac{R_H}{\frac{V_{OUT}}{0.6} - 1}$$



Input Capacitor

The input capacitor is used to supply the AC input current to the step-down converter and maintain the DC input voltage. The capacitors must have a ripple current rating that exceeds the converter's maximum input ripple current. The RMS ripple current through the input capacitor can be calculated by:

$$I_{CIN} = I_{OUT} * \sqrt{\frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

where I_{OUT} is the load current, V_{OUT} is the output voltage, V_{IN} is the input voltage.

Thus, the input capacitor can be calculated by the following equation when the input ripple voltage is determined.

$$C_{IN} = \frac{I_{OUT}}{F_{SW} * \Delta V_{IN}} * \frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where C_{IN} is the input capacitance value, F_{SW} is the switching frequency, ΔV_{IN} is the input ripple voltage.

The input capacitor can be electrolytic, tantalum or ceramic. To minimizing the potential noise, a small X5R or X7R ceramic capacitor, e.g., 0.1μF, should be placed as close to the IC as possible when using electrolytic capacitors. 3x10μF/25V ceramic capacitors are recommended in typical application.

Output Capacitor

The output capacitor is required to maintain the DC output voltage, and the capacitance value determines the output ripple voltage. The output voltage ripple can be calculated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} * L} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right) * \left(R_{ESR} + \frac{1}{8 * F_{SW} * C_{OUT}}\right)$$

where C_{OUT} is the output capacitance value and R_{ESR} is the equivalent series resistance value of the output capacitor.

The output capacitor can be low ESR electrolytic, tantalum or ceramic, which lower ESR capacitors get lower output ripple voltage.

The output capacitors also affect the system stability and transient response, and at least 5x47μF ceramic capacitors are recommended in typical application.

Inductor

The inductor is used to supply constant current to the output load, and the value determines the ripple current which affect the efficiency and the output voltage ripple. The ripple current is typically allowed to be 40% of the maximum switch current limit, thus the inductance value can be calculated by:

$$L = \frac{V_{OUT}}{F_{SW} * \Delta I_L} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where V_{IN} is the input voltage, V_{OUT} is the output voltage, F_{SW} is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

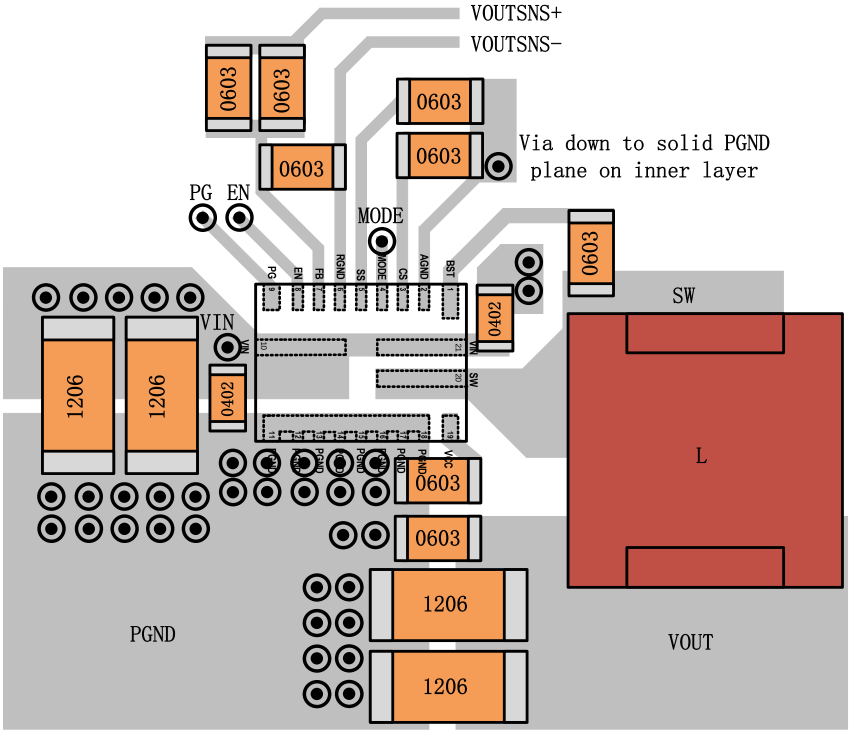
External Bootstrap Capacitor

The bootstrap capacitor is required to supply voltage to the top switch driver. A 0.1μF low ESR ceramic capacitor is recommended to connected to the BST pin and SW pin.

PCB Layout Note

The PCB layout is critical for best operating performance, follow the guidelines as below.

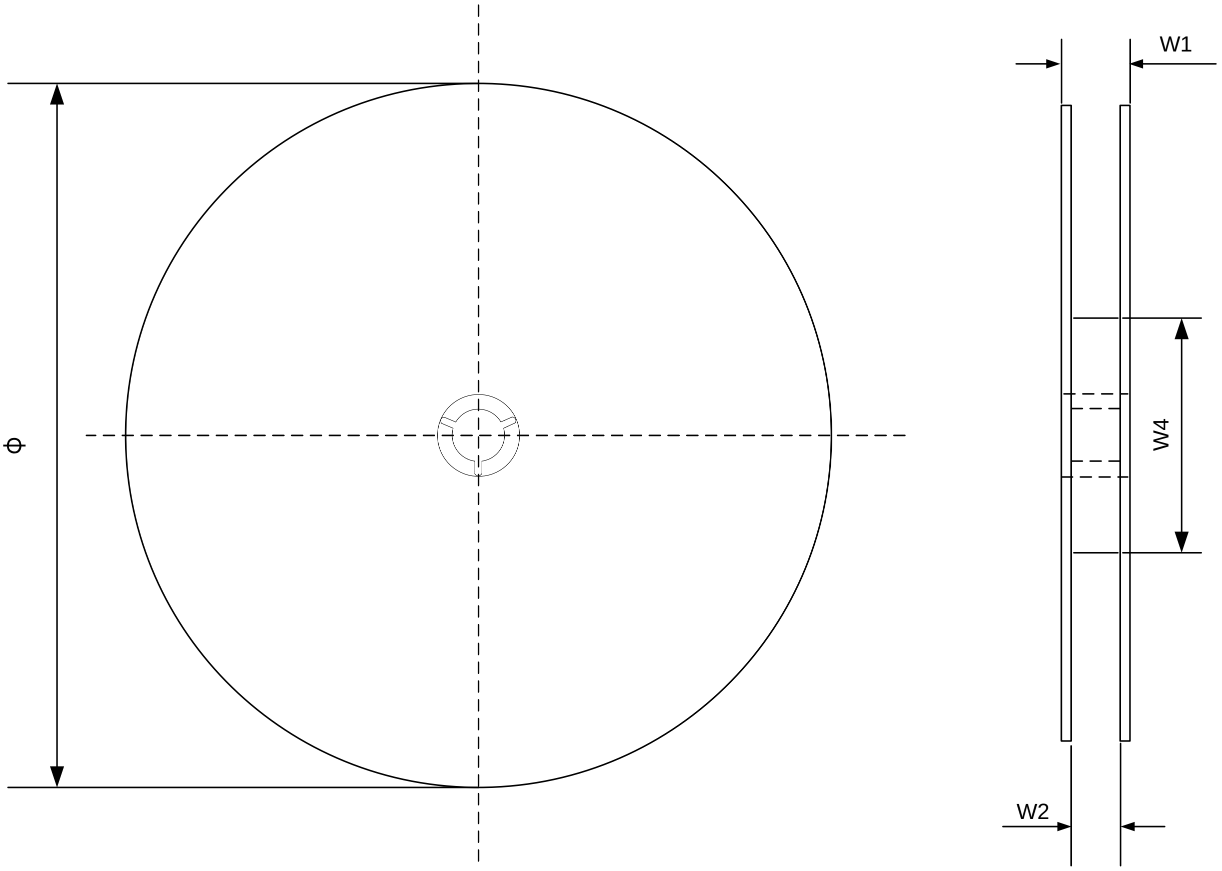
1. Place the input decoupling capacitor as close to device (VIN pin and PGND) as possible to eliminate noise at the input pin. The loop area formed by input capacitor and GND must be minimized.
2. A solid ground inner plane is recommended to isolate the signal traces from noisy power traces.
3. AGND Pin (Pin 2) is recommended to be connected to a solid PGND plane on inner layer.
4. If a solid PGND plane on inner layer is not available for PCB design, it is highly recommended to connect the AGND to the point of the VOUT capacitor’s ground directly. Alternatively, connect AGND and PGND at the point of the VCC capacitor’s ground, and place output capacitors close to VCC decoupling capacitor, then make the PGND connection using an entire copper plane on top layer.
5. Place as many PGND vias as possible and make the ground plane as large as possible to optimize heat dissipation and parasitic impedance.
6. Place the VCC decoupling capacitor as close as possible to the device.
7. Place the BST capacitor as close as possible to the BST and SW pins. 20mil or wider traces are recommended for the connection.
8. Place the feedback resistors close to device to minimize the feedback trace, and put the feedback trace far away from the inductor and noisy power traces like SW node. It is recommended to shield the pair of remote sensing traces with ground planes above and below.
9. Keep the switching node SW short to prevent excessive capacitive coupling.
10. Make VIN, VOUT and ground bus connections as wide as possible to reduce voltage drop on the input and output paths of the converter and maximize efficiency.



PCB Layout Recommendation

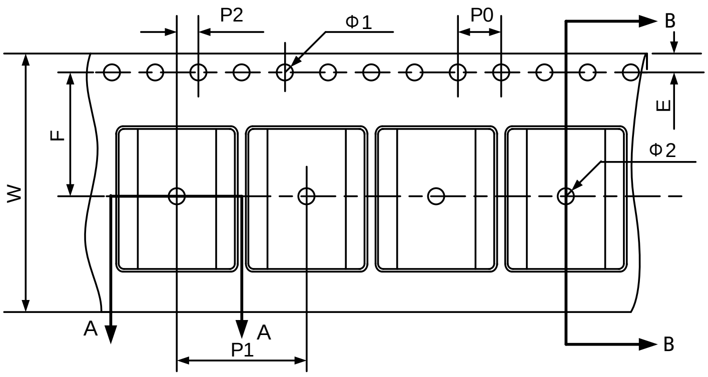
TAPE AND REEL INFORMATION

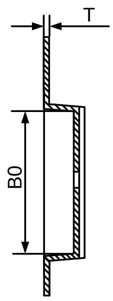
Reel UNIT: mm



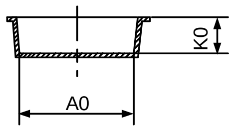
Package	Diameter Φ	Thickness W1	Width W2	W4
QFN3*4-21	330±2	17.6±2	12.4±2	100±2

Carrier Tape UNIT: mm





SECTION B-B



SECTION A-A

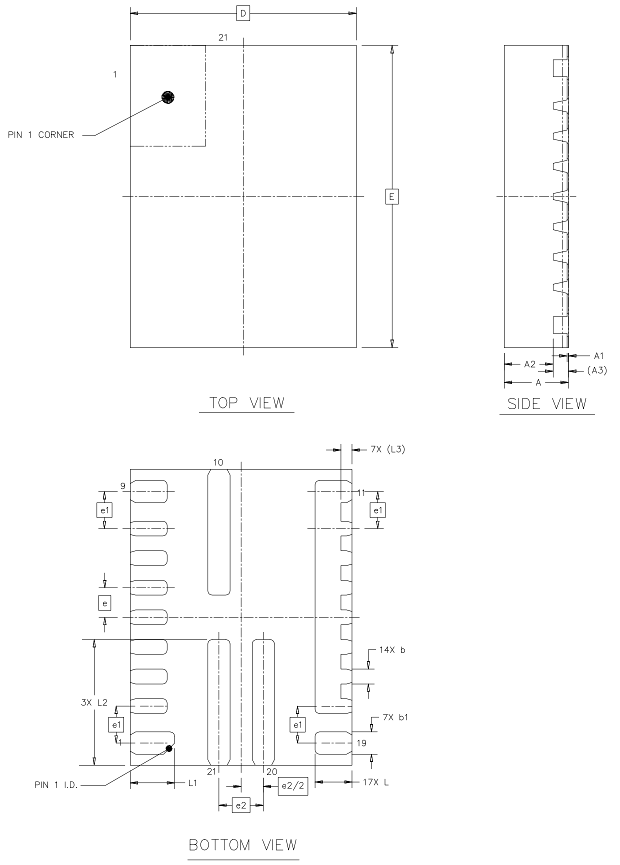
Note :

1) The carrier type is black, and colorless transparent.
2) Carrier camber is within 1mm in 100mm.
3) 10 pocket hole pitch cumulative tolerance:±0.20.
4) All dimensions are in mm.

Package	Tape dimensions (mm）											
	P0	P2	P1	A0	B0	W	T	K0	Φ1	Φ2	E	F
QFN3*4-21	4.0±0.1	2.0±0.1	8.0±0.1	3.30±0.2	4.30±0.2	12±0.3	0.25±0.1	1.1±0.15	1.5±0.10	1.55±0.1	1.75±0.1	5.50±0.10

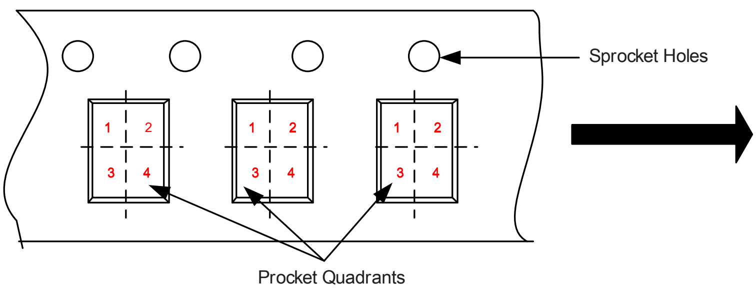
PACKAGE OUTLINE

QFN3X4-21 UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2	—	0.65	—
A3	0.203 REF		
b	0.15	0.20	0.25
b1	0.25	0.30	0.35
D	2.90	3.00	3.10
E	3.90	4.00	4.10
e	0.40 BSC		
e1	0.50 BSC		
e2	0.60 BSC		
L	0.40	0.50	0.60
L1	0.50	0.60	0.70
L2	1.60	1.70	1.80
L3	0.15 REF		

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE



Package Type	Pin1 Quadrant
QFN3X4-21	1

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