JWH5084

17V/12A

Sync. Step-Down Converter

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW®H5084 is a monolithic buck switching regulator based on I2 architecture for fast transient response. Operating with an input range of 4.5V~17V, JWH5084 delivers 12A of continuous output current with two integrated N-Channel MOSFETs. The internal synchronous power switches provide high efficiency without the use of an external Schottky diode. The operation frequency is set easily to 400 kHz, 800 kHz, or 1200 kHz with the MODE configuration, allowing the JWH5084 frequency to remain constant regardless of the input/output voltages. JWH5084 guarantees robustness with output short protection, over-voltage protection, thermal protection and under voltage protection.

JWH5084 is available in QFN3.5 X 3.5-18 package, which provide a compact solution with minimal external components.

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FEATURES

- 4.5V to 17V operating input range
- 12A continuous
- Selectable accurate current limit level
- $\pm$1% reference voltage over -40℃ to +125℃ junction temperature range
- Selectable PFM or FCCM
- Power good indicator
- Programmable soft-start time
- Selectable switching frequency from 400kHz, 800kHz, and 1200kHz
- Output discharge function
- Non-latch OCP, UVP, OVP, UVLO, Thermal protection
- Available in QFN3.5X3.5-18 package

APPLICATIONS

- Telecom and Networking Systems
- Server, Cloud-Computing, Storage
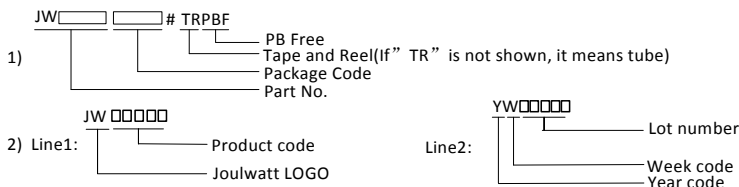- Base Stations
- General Purpose Point-of-Load
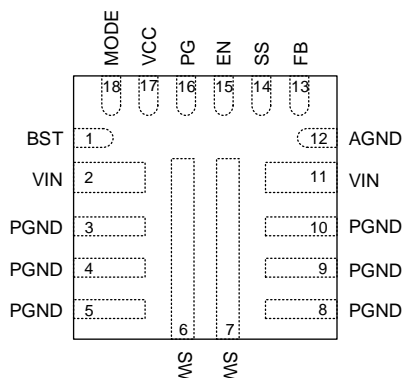
TYPICAL APPLICATION
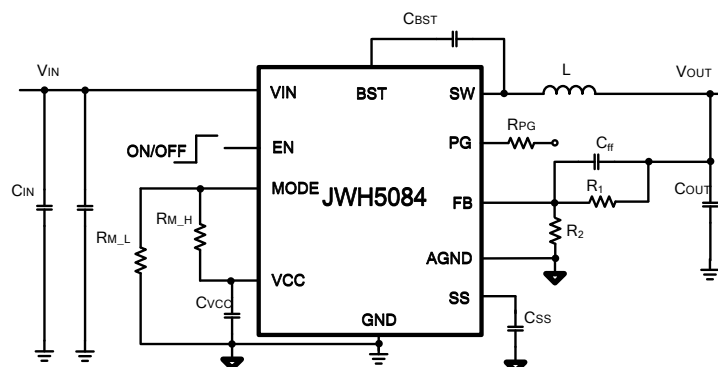
ORDER INFORMATION

DEVICE[1]	PACKAGE	TOP MARKING[2]
JWH5084QFNZ#TRPBF	QFN3.5X3.5-18	JWH5084 YW☐☐☐☐☐

Notes：

1) JW☐☐ ☐# TRPBF
   - PB Free
   - Tape and Reel(If"TR"is not shown, it means tube)
   - Package Code
   - Part No.

2) Line1: JW☐☐☐☐☐
   - Product code
   - Joulwatt LOGO

   Line2: YW☐☐☐☐
   - Lot number
   - Week code
   - Year code

PIN CONFIGURATION

TOP VIEW

ABSOLUTE MAXIMUM RATING[1]

VIN Pin.. -0.3V to 20V

SW Pin... -0.3V (-5V for 25ns) to 20V (25V for 25ns)

EN Pin……………………………………………………………………………….…………………………-0.3V to   20V

BST Pin .... SW-0.3V to SW+4V

VCC Pin .... -0.3V to 4V

PG Pin .... -0.3V to 6V

All other Pins .... -0.3V to 4V

Junction Temperature [2] 150ºC

Lead Temperature 260ºC

ESD Susceptibility (Human Body Model) .... ±2kV

Charged device model (CDM), per JEDEC specification JESD22- V C101.................................... ±500V

RECOMMENDED OPERATING CONDITIONS[3)]

Input Voltage VIN .... 4.5V to 17V

Output Voltage Vout .... 0.6V to 5.5V

Maximum Output Current I_{OUT_MAX} 12A

Operation Junction Temperature T_j.. .... -40°C to 125°C

THERMAL PERFORMANCE[4)]　　　　　　　　　　　θ_{JB} [5)]　θ_{Jc_TOP} [5)]

QFN3.5X3.5-18...8.6....17.0ºC/W

Note：

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDE OPERATING CONDITIONS.

2) The JWH5084 includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The device is not guaranteed to function outside its operating conditions.

4) Measured on JESD51-7, 4-layer PCB.

5) θ_{JB} Thermal resistance from junction to board around PGND pin soldering point.

   θ_{Jc_TOP} Thermal resistance from junction to top of package.

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ELECTRICAL CHARACTERISTICS

VIN=12V, T$_J$=-40℃~125℃，Unless otherwise stated.						
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
V$_{IN}$ Under Voltage Lock-out Threshold	V$_{IN\_HTH}$	V$_{IN}$ rising, V$_{CC}$=3.3V	2.1	2.4	2.7	V
	V$_{IN\_LTH}$	V$_{IN}$ falling, V$_{CC}$=3.3V	1.55	1.85	2.15	V
Shutdown Current	I$_{SD}$	V$_{EN}$=0		7		µA
Supply Current	I$_Q$	V$_{EN}$=3.3V, V$_{FB}$=0.7V		550	800	µA
Enable Input Rising Threshold	V$_{EN\_HTH}$		1.17	1.225	1.27	V
Enable Hysteresis	V$_{EN\_TH\_HYS}$			0.121		V
I$_{ENP1}$	EN pull-up	V$_{EN}$=1.0V	0.35	1.91	2.95	µA
I$_{ENP2}$	current	V$_{EN}$=1.3V	3	4.197	5.5	µA
Feedback Voltage	V$_{REF}$		594	600	606	mV
Top Switch Resistance	R$_{DS(ON)T}$			13.3	21	mΩ
Bottom Switch Resistance	R$_{DS(ON)B}$			4.3	8.4	mΩ
Top Switch Leakage Current	I$_{LEAK\_TOP}$	V$_{IN}$=17V, V$_{SW}$=0V			10	µA
Bottom Switch Leakage Current	I$_{LEAK\_BOT}$	V$_{IN}$=17V, V$_{SW}$=17V			10	µA
Valley current limit	I$_{LIM\_POS1}$		9.775	11.5	13.225	A
	I$_{LIM\_POS2}$		11.73	13.8	15.87	A
Bottom Switch Negative Current Limit	I$_{LIM\_NEG}$			-4		A
Minimum On Time[6]	T$_{ON\_MIN}$			50		ns
Minimum Off Time	T$_{OFF\_MIN}$			100	180	ns
Switching Frequency [7]	F$_{SW}$		340	400	460	kHz
			680	800	920	kHz
			1020	1200	1380	kHz
Discharge FET Ron	R$_{DIS}$			80	150	Ω
Soft-Start Charge Current	I$_{SS\_CHAR}$	V$_{SS}$=0V	4.9	6	7.1	µA
Soft-Start Discharge FET Ron	R$_{SS\_DISCHAR}$	V$_{CC}$=3V	1	1.5	2	kΩ
Soft-Start Time[6]	T$_{SS}$	Internal soft-start time		1		ms
VCC Under-voltage Lockout Threshold	V$_{CC\_HTH}$	VCC rising	2.65	2.8	2.95	V
	V$_{CC\_LTH}$	VCC falling	2.35	2.5	2.65	V
VCC Regulator	V$_{CC}$		3.28	3.38	3.48	V
VCC Load Regulation		I$_{CC}$=25mA		0.5		%
Power Good High Threshold	PG$_{HTH}$	FB from low to high	90%	93%	96%	V$_{REF}$
		FB from high to low	104%	107%	110%	V$_{REF}$
Power Good Low Threshold	PG$_{LTH}$	FB from low to high	113%	116%	119%	V$_{REF}$

VIN=12V, T_J=-40℃~125℃，Unless otherwise stated.

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
		FB from high to low	81%	84%	87%	V_{REF}
Power Good Delay Time	PG_DLY	PG from low to high	140	200	260	us
Power Good Sink Current	I_{PG}	PG=0.5V	10			mA
Output Over-voltage Threshold		V_{FB} Rising	118%	121%	124%	V_{REF}
Output Under-voltage Threshold[6]		V_{FB} Falling	65%	68%	71%	V_{REF}
Thermal Shutdown[6]	T_{TSD}			160		°C
Thermal Shutdown Hysteresis[6]	T_{TSD_HYST}			15		°C
VCC Regulator Thermal Shutdown[6]				171		°C
VCC Regulator Thermal Shutdown Hysteresis[6]				18		°C

Note：

6) Guaranteed by design.

7) Guaranteed by design over all temperature range

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PIN DESCRIPTION

Pin	Name	Description
1	BST	Connect a 0.1uF capacitor between BST and SW pin to supply current for the top switch driver.
2,11	VIN	Input voltage pin. VIN supplies power to the IC. Connect a 4.5V to 17V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC
3,4,5,8,9,10	GND	Power ground pin
6,7	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
12	AGND	Analog ground pin. Select AGND as the control circuit reference point.
13	FB	Feedback. An external resistor divider from the output to AGND (tapped to FB) sets the output voltage. It is recommended to place the resistor divider as close to FB as possible. Vias should be avoided on the FB traces.
14	SS	Soft-start time setting pin. The soft-start time is determined by the capacitance between SS pin and AGND.
15	EN	Enable control pin. Pull this pin high to turn on the regulator. Do not leave this pin floating.
16	PGOOD	Power good monitor output. Open drain output when the output voltage is within 93% to 116% of internal reference voltage.
17	VCC	Internal LDO Output. Power supply for internal analog circuits and driving circuit. Decouple this pin to ground with a minimum 1uF ceramic capacitor.
18	MODE	Operation mode selection. Program MODE to select CCM, pulse skip mode, the operating switching frequency, and current limit selection.

BLOCK DIAGRAM

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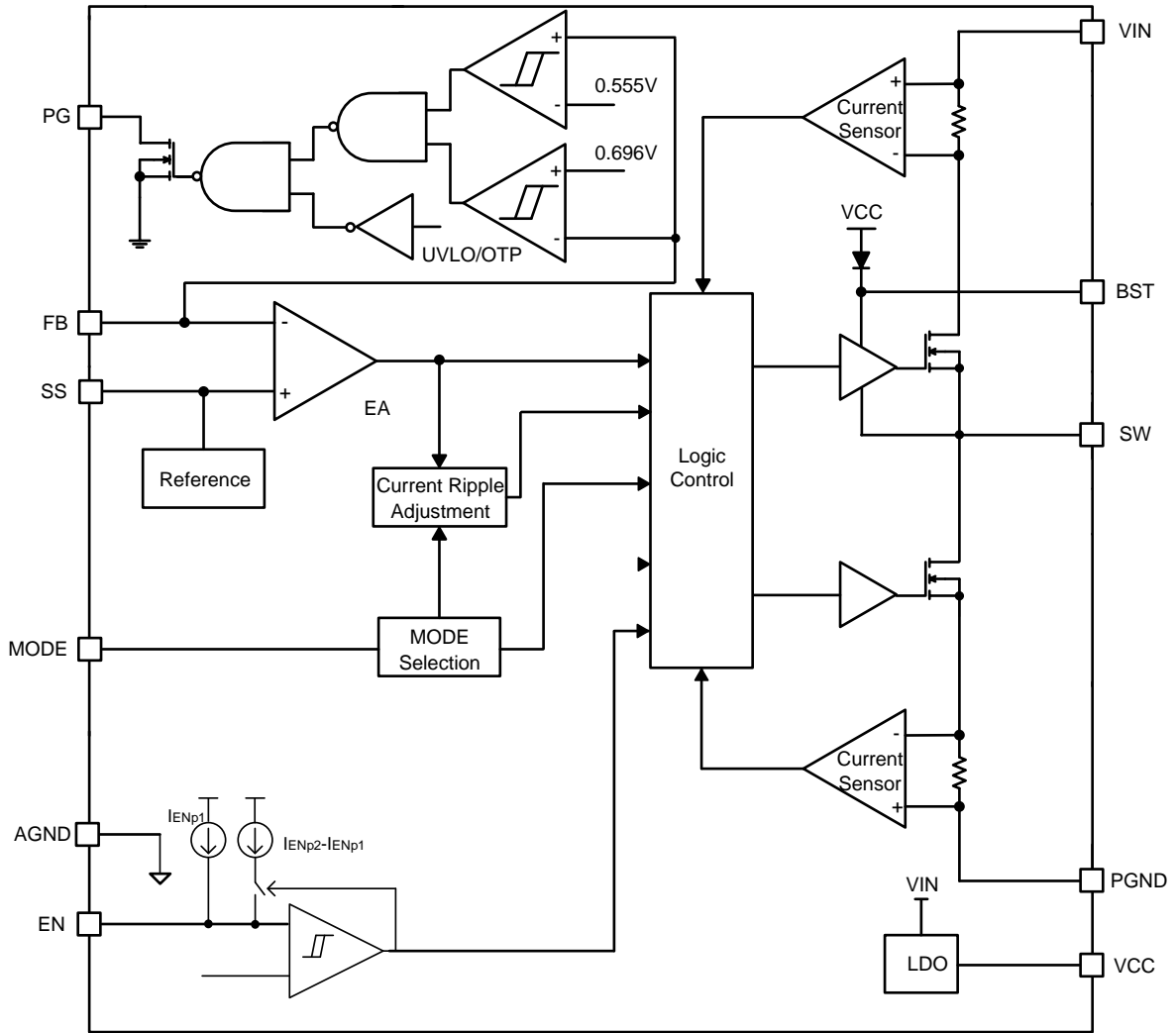
FUNCTIONAL DESCRIPTION

JWH5084 is a synchronous step-down regulator based on I2 control architecture. It regulates input voltages from 4.5V to 17V down to as low as 0.6V output voltage, and is capable of supplying up to 12A of load current.

Power Switch

N-Channel MOSFET switches are integrated on the JWH5084 to down convert the input voltage to the regulated output voltage. Since the top MOSFET needs a gate voltage greater than the input voltage, a boost capacitor connected between BST and SW pins is required to drive the gate of the top switch. The boost capacitor is charged by the internal LDO when SW is low.

CCM Operation

Continuous conduction mode (CCM) occurs when the output current is high, and the inductor current is always above zero amps. The JWH5084 can also be configured to operate in forced CCM operation when the output current is low (See *Mode Selection* section for details). In CCM operation, the switching frequency is fairly constant; hence the output ripple keeps almost the same throughout the whole load range.

PFM Operation

At light load condition, theJWH5084 can be configured to work in PFM mode to optimize the efficiency. When the load decreases, the inductor current will decrease as well. Once the inductor current reaches zero, the part transitions from CCM to PFM mode if the JWH5084 is configured so (see *Mode Selection* section for details).

In PFM mode operation, the high side MOSFET

is turned off by the peak current reference and the low side MOSFET turns on until the inductor current reaches zero. At this time, the output voltage is still higher than the target value which causes the internal COMP voltage lower than a clamp value, and the high side MOSFET is not allowed to turn on until the COMP voltage rises above its clamp voltage.

At light load condition, the high side MOSFET is not turned on as frequently in PFM mode as it is in forced CCM. As a result, the efficiency in pulse skip mode is improved greatly, comparing with that in forced CCM operation.

As the output current increases from the light load condition, the time period within which the current modulator regulates becomes shorter. The high side MOSFET is turned on more frequently. Hence, the switching frequency increases accordingly. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current is determined with the following equation:

$$I_{OUT} := \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{2 \cdot L \cdot f_{SW} \cdot V_{IN}}$$

The part enters PWM mode once the output current exceeds the critical level. After that, the switching frequency stays fairly constant over the output current range.

Mode Selection

The JWH5084 provides both forced CCM operation and PFM mode operation in a light-load condition. The JWH5084 has three options for switching frequency selection. Selecting the operation mode under light load condition and the switching frequency is done

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by choosing the resistance value of the resistor connected between MODE and AGND or VCC (See Table 1).

Table 1 --- MODE selection

R_{M_L} (KΩ)	R_{M_H} (KΩ)	Mode	Current limit	Fs
5.1	300	FCCM	I_{LIM_POS1}	400k
10	200	FCCM	I_{LIM_POS2}	400k
20	160	FCCM	I_{LIM_POS1}	800k
20	120	FCCM	I_{LIM_POS2}	800k
51	200	FCCM	I_{LIM_POS1}	1200k
51	180	FCCM	I_{LIM_POS2}	1200k
51	150	PFM	I_{LIM_POS1}	400k
51	120	PFM	I_{LIM_POS2}	400k
51	91	PFM	I_{LIM_POS1}	800k
51	82	PFM	I_{LIM_POS2}	800k

Shut-Down Mode

The JWH5084 shuts down when voltage at EN pin is below 0.3V. The entire regulator is off and the supply current consumed by the JWH5084 drops below 7uA.

VIN Under-Voltage Protection

In addition to the enable function, the JWH5084 provides an Under Voltage Lock-out (UVLO) function that monitors the input voltage. To prevent operation without fully-enhanced internal MOSFET switches, this function inhibits switching when input voltage drops below the UVLO-falling threshold. The IC resumes switching when input voltage exceeds the UVLO-rising threshold.

Enable and Adjustable UVLO Protection

The JWH5084 is enabled when the VIN pin voltage rises above 2.4V and the EN pin

exceeds the enable threshold of 1.22V. The JWH5084 is disabled when the VIN pin voltage falls below 1.85V or when the EN pin voltage is below around 1.1V. Do not leave this pin floating.

If an application requires a different turn-on and turn-off thresholds respectively, use a resistive divider connected between VIN and ground with the central tap connected to EN to adjust the input voltage UVLO. (Shown in Figure 1). The EN pin has a pull-up current I_{ENP1} that sets the default state of the pin when it is floating. This current increases to I_{ENP2} when the EN pin voltage crosses the turn-on threshold. The UVLO thresholds can be set by following equation:
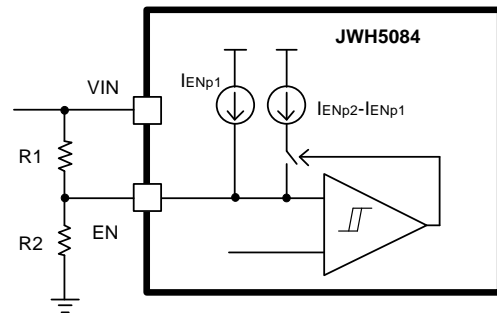

Fig. 1 Adjustable UVLO

The input voltage UVLO threshold (V_{UVLO}) and hysteresis (V_{UVLO_HYS}) can be calculated by the following equation.

$$R_1 = \frac{V_{START} \times \frac{V_{EN\_LTH}}{V_{EN\_HTH}} - V_{STOP}}{I_{ENP1}\left(1 - \frac{V_{EN\_LTH}}{V_{EN\_HTH}}\right) + \left(I_{ENP2} - I_{ENP1}\right)}$$

$$R_2 = \frac{R_1 \times V_{EN\_HTH}}{V_{START} + \left(R_1 \times I_{ENP1}\right) - V_{EN\_HTH}}$$

where
V_{EN_HTH} = 1.225V
V_{EN_LTH} = 1.104V
I_{ENP2} = 4.197uA
I_{ENP1} = 1.91uA

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Soft Start

Soft-start is designed in JWH5084 to prevent the converter output voltage from overshooting during startup and short-circuit recovery. An internal current source (I_{SS}) of 6uA is designed to charge the external soft-start capacitor (C_{SS}) and generates a soft-start (SS) voltage ramping up from 0V to 1.5V. When it is less than internal reference voltage (V_{REF}, typ. 0.6V), SS voltage overrides V_{REF} and the error amplifier uses SS voltage as the reference. When SS exceeds V_{REF}, V_{REF} regains control.

The soft start time (10% to 90%) T_{SS} can be calculated by the following equation.

$$T_{SS}(ms) := \frac{C_{SS}(nF) \cdot V_{REF}(V) \cdot 0.8}{I_{SS}(\mu A)}$$

where C_{SS} is the soft-start capacitance connected between SS pin and AGND pin.

At power up, the soft start pin is discharged before MOSFETs switching to ensure a proper power up. Also, during normal operation, the JWH5084 will stop switching and the soft-start pin will be discharged, when the VIN UVLO is exceeded, EN pin pulled below 1.1V, or a thermal shutdown event occurs.

Current Sense and Over-Current Protection (OCP)

The JWH5084 features an on-die current sense and two programmable positive current limit thresholds.

The current limit is active when the JWH5084 is enabled. During the low side MOSFET on state, the SW current (inductor current) is sensed, and compared with current limit cycle-by-cycle. The high side MOSFET is only allowed to turn on when the sensed current is below the internal OCP threshold I_{LIM} (during the low side MOSFET on state) to limit the SW valley current cycle-by-cycle.

The OCP HICCUP is active during soft start, once OCP HICCUP is active, if the JWH5084 detects over-current condition for consecutive 1000 cycles, it enters HICCUP mode. After soft start, when the current is limited by OCP, the output voltage tends to drop, if the FB drops below under-voltage protection (UVP) threshold for 1ms, it enters HICCUP mode. In HICCUP mode, the JWH5084 latches off the high side MOSFET immediately, and latches off low side MOSFET. Meanwhile, the SS capacitor is also discharged. After about 31ms, the JWH5084 will try to soft start automatically. If the over-current condition still holds, the JWH5084 repeats this operation cycle until the over-current condition disappears, and the output voltage rises smoothly back to the regulation level.

Negative Inductor Current limit

When the low side MOSFET detects a -4A current, the part turns off the low side MOSFET to limit the negative current.

Pre-Bias Start-Up

The JWH5084 has been designed for a monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the IC disables switching for both the high-side and low-side MOSFETs until the voltage on the SS capacitor exceeds the sensed output voltage at FB. Before SS voltage reaches pre-biased FB level, if the BST voltage (from BST to SW) is lower than 1.8V, the low-side MOSFET is turned on to allow the BST voltage to be charged through VCC. The low-side MOSFET is turned on for very narrow pulses, so the drop in pre-biased level is negligible.

Output Voltage Discharge

When the JWH5084 is disabled through EN, it

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enables the output voltage discharge mode. This causes both the high side MOSFET and the low side MOSFET to latch off. A discharge FET connected between SW and PGND is turned on to discharge the output voltage. The typical switch on resistance of this FET is about 80Ω. Once the FB voltage drops below 10%* V_{REF}, the discharge FET is turned off.

Output Over-voltage Protection

The JWH5084 monitors the output voltage by connecting FB to the tap of the output voltage feedback resistor divider to detect an overvoltage condition. This provides auto-recovery OVP mode.

In PFM mode, if the FB voltage exceeds 109% of the REF voltage, the low side MOSFET is turned on until it hits the low-side negative current limit (NOCP). Once it hits NOCP, the low side MOSFET is turned off and the high side MOSFET is turned on. If the FB voltage is still higher than 104% of REF voltage, the low side MOSFET is then turned on again. The JWH5084 keeps this operation until the FB voltage drops below 104% of the REF voltage. Once it does, the JWH5084 exit this mode, the low side MOSFET is allowed to turn off for PFM operation. If FB rises back to more than 109% of the REF voltage, the low side MOSFET turns on again until FB drops back below 104% of the REF voltage.

Power Good

The JWH5084 has power-good (PG) output. The PG pin is the open drain of a MOSFET. Connect to VCC or another voltage source through a resistor. After applying the input voltage, the MOSFET turns on, so PG is pulled to GND before SS is ready. After the FB voltage reaches 93% of the REF voltage, PG is pulled

high after a certain time elapsed.

When the FB voltage drops to 84% of the REF voltage, PG is pulled low. When the FB voltage rises above 93% of the REF voltage, PG is pulled high again.

When the FB voltage exceeds 116% of the REF voltage, PG is pulled low. When the FB voltage drops to 107% of the REF voltage, PG is pulled high again.

Once EN UVLO, OVP, UVP or OTP is triggered, PG is pulled low within 1us deglitch time.
If the input supply fails to power the JWH5084, PG is clamped low even though PG is tied to an external DC source through a pull-up resistor. The relationship between the PG voltage and the pull-up current is shown in Figure 2 below:
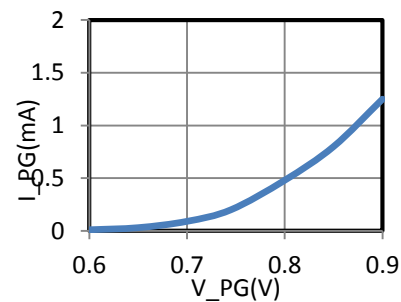

Fig. 2 Power Good clamped voltage vs. pull-up current

Thermal Protection

When the temperature of the JWH5084 rises above 160°C, it is forced into thermal shut-down. This is a non-latch protection, the regulator becomes active again when the temperature goes below the thermal shutdown threshold.
There is a second higher thermal protection, the threshold is at typically 171°C. The internal LDO will shut down once temperature goes beyond 171°C. The LDO re-starts working when the temperature goes below the second thermal shutdown threshold.

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PACKAGE OUTLINE

QFN3.5X3.5-18 | UNIT: mm

TOP VIEW

SIDE VIEW

BOTTOM VIEW

(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2	—	0.65	—
A3	0.203REF		
b	0.20	0.25	0.30
b1	0.25	0.30	0.35
b2	0.35	0.40	0.45
D	3.50BSC		
E	3.50BSC		
e	0.50BSC		
e1	0.55BSC		
e2	0.60BSC		
e3	0.65BSC		
e4	0.575BSC		
e5	0.30BSC		
L	0.30	0.40	0.50
L1	0.85	0.95	1.05
L2	2.30	2.40	2.50

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE

Sprocket Holes

Procket Quadrants

Package Type	Pin1 Quadrant
QFN3.5X3.5-18	1

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