

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW[®]7203 is a low side ideal diode and ORing controller that drives one external N-channel MOSFET. Forming the diode-OR with N-channel MOSFET instead of Schottky diode reduces power consumption, heat dissipation and PC board area.

With the JW7203, power sources can easily be ORed together to increase total system reliability.

In the forward direction the JW7203 controls the voltage drop across the MOSFET to ensure smooth current transfer from one path to the other without oscillation. If a power source fails or is shorted, fast turnoff minimizes reverse current transients.

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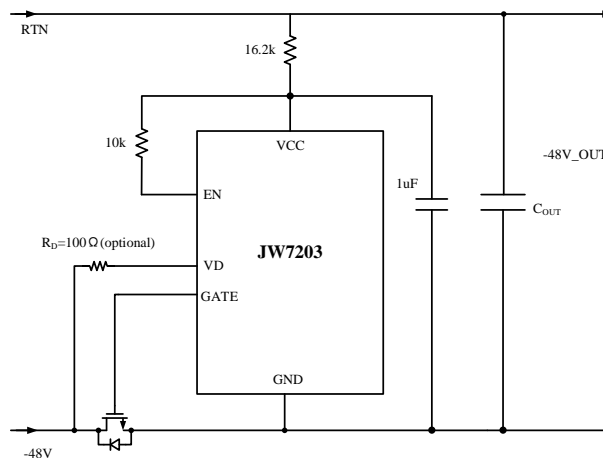
FEATURES

- Replaces Power Schottky Diode
- Controls N-Channel MOSFET
- 200V Absolute Maximum
- 0.3 μ s Turn-Off Time Limits Peak Fault Current
- Smooth Switchover without Oscillation
- No Reverse DC Current
- Regulation: 25 mV \pm 15 mV
- Fast Turn off: -25 mV \pm 15 mV
- Available in 8-Lead SOP Packages

APPLICATIONS

- High Availability Systems
- Advanced TCA[®] (ATCA) Systems
- \pm 48V Distributed Power Systems
- Computer Systems/Servers
- Telecom Infrastructure
- Optical Networks

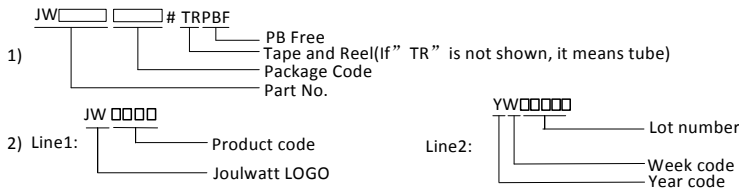
TYPICAL APPLICATION



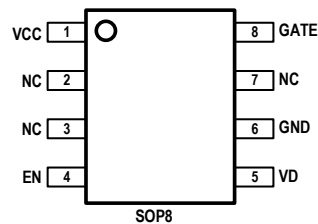
ORDER INFORMATION

DEVICE ¹⁾	PACKAGE	TOP MARKING ²⁾
JW7203SOPB#TRPBF	SOP8	JW7203 YW□□□□□

Note:



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATING^{1) 2)}

Supply Voltage--- V_{VCC} (current into V_{CC} < 10 mA).....	-0.3V to 20V
Input Voltage--- V_D	-1V to 200V
Input Voltage--- V_{EN}	0V to 30V
Output voltage--- V_{GATE}	-0.5V to V_{CC}
Operating junction temperature, T_J	-40°C to 125°C
Storage temperature, T_{stg}	-55°C to 150°C

RECOMMENDED OPERATING CONDITIONS

V _{VCC} ---External supply voltage.....	0V to 13.5V
V _{VCC} ---Internal clamp voltage (current into V _{CC} <10 mA).....	0V to 18V
V _{EN}	0V to V _{CC}
V _D	-0.2V to 150V
V _{GATE}	0V to V _{CC}
R _{VD}	0 Ω to 1kΩ

THERMAL PERFORMANCE⁴⁾

	θ_{JA}	θ_{JC}
SOP8.....	116.....	62°C/W

Note:

- 1) Exceeding these ratings may damage the device.
- 2) All currents into pins are positive, all voltage are referenced to GND unless otherwise specified.
- 3) The GATE pins are internally limited to a minimum of 13.5V above VCC. Driving these pins beyond the clamp may damage the part.
- 4) Measured on JESD51-7, 4-layer PCB

ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $1.1\text{ mA} < I_{VCC} < 10\text{ mA}$, $-1\text{V} < V_D < 150\text{ V}$; $EN=2\text{V}$; All pin voltages are relative to GND (unless otherwise noted).

Item	Symbol	Condition	Min.	Typ.	Max.	Units
VCC						
UVLO on VCC	$V_{(UVLO_VCC)}$	rising	9	9.5	10	V
UVLO hysteresis on VCC	$V_{(UVLO_VCC, hyst)}$	hysteresis		1.2		V
VCC internal regulator voltage	$V_{(VCC_INT)}$	$1.1 < I_{(VCC)} < 10\text{ mA}$ (current into V_{CC})	12	14.5	18	V
VCC external supply voltage	$V_{(VCC_EXT)}$		10		13.5	V
Quiescent Current	Quiescent Current	$V_{VCC} = 10\text{ V}$, On			1	mA
		$V_{VCC} = 10\text{ V}$, GATE in regulation			1.1	
EN						
Threshold voltage for V_{EN}	V_{EN_rising}		0.97	1	1.03	V
Hysteresis current. Sourcing from EN pin	I_{EN_hyst}	$V_{EN}=1.5\text{V}$	8	10	12	μA
V_D						
Leakage current	$I_{(I_{kg,D})}$	$V_D = -50\text{ mV}$, GATE ON	-2		2	μA
		$V_D = -100\text{ mV}$, GATE ON	-7		7	
		$V_D = 150\text{ V}$, GATE off			30	
Forward regulation voltage of the ORing controller. $V_{FWD} = GND - V_D$	$V_{(FWD)}$		10	25	40	mV
Forward voltage where a fast pull up is activated.	$V_{(FWD,FST)}$	GATE = 5 V. $GND - V_D \uparrow$ measure when $I_{GATE} = 100\ \mu\text{A}$	50	80	105	mV
Fast reverse trip voltage.	$V_{(RV)}$		10	25	40	mV
Response time to large reverse current ⁵⁾	$T_{VD,FST,RESP}$	V_D steps from -40 mV to 15 mV. Measure time for GATE to come down.		300		ns
GATE						
Gate Output Voltage	$V_{VCC-GATE}$			0.65	1.1	V
Gate sourcing current in regulation	$I_{(GATE,SRS)}$	$GND - V_D = 50\text{ mV}$		30		μA
Gate sinking current in regulation	$I_{(GATE,SINK)}$	$GND - V_D = 0$		30		μA
Pull up resistance in fast sourcing mode.	$R_{GATE, SRC, FS}$ T	$GND - V_D = 100\text{ mV}$; Measure current at $V_{GATE} = 0\text{ V}$. $R = V_{VCC}/I$		17		$\text{k}\Omega$
Fast Gate pull down current	$I_{(GATE,FST)}$	$GND - V_D = -15\text{ mV}$	0.4	1	1.5	A
OTSD (Over Temperature Shut Down)						

Shutdown temperature ⁵⁾	T _{SD}	Temp Rising		155		°C
Shutdown temperature Hysteresis ⁵⁾	T _{SD,hyst}			8		°C

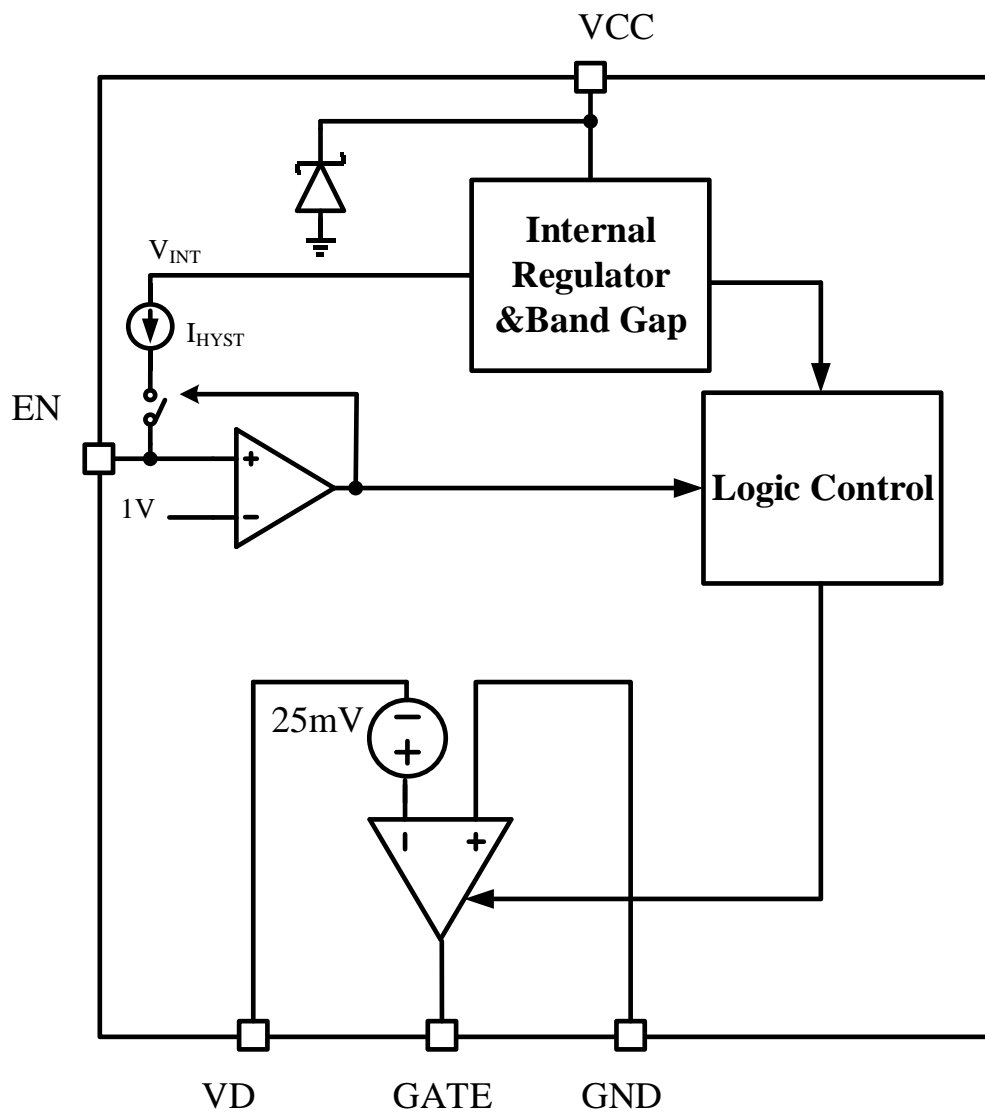
Note:

5) Guaranteed by design.

PIN DESCRIPTION

Name		Description
SOP-8	Pin	
1	VCC	Power supply. Tied to external power through a resistor. A 0.1uF or larger ceramic cap is recommended close to this pin.
2	NC	No connect.
3	NC	No connect.
4	EN	Enable pin. Drive EN high to turn on controller and drive EN low to turn off the controller.
5	VD	Connected to drain of FET. The JW7203 will regulate the drop from GND to D to 25 mV to mimic an ideal diode.
6	GND	This pin corresponds to the IC GND.
7	NC	No connect.
8	GATE	Gate driver for the ORing FET.

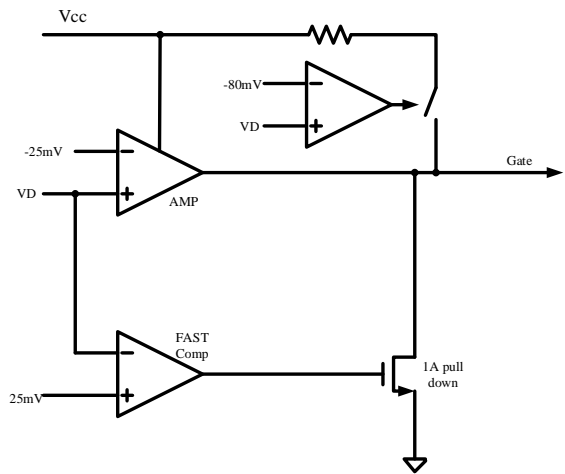
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The JW7203 is an integrated Single ORing controller that enables high power telecom systems to comply with stringent transient requirements. ORing diodes have been a popular means of connecting these supplies at the point of load. The disadvantage of this approach is the forward voltage drop and resulting efficiency loss. This drop reduces the available supply voltage and dissipates significant power. Using N-channel MOSFETs to replace Schottky diodes reduces the power dissipation and eliminates the need for costly heat sinks or large thermal layouts in high power applications.

The JW7203 is a low side ideal diode and ORing controller that drives one external N-channel MOSFET as pass transistor to replace ORing diode. The GND and VD pins form the anode and cathode of the ideal diode. The source pin of the external MOSFET is connected to the GND pin. The drain of the MOSFET is connected at the VD pin. The gate of the external MOSFET will be driven by the JW7203 to regulate the voltage drop across the pass transistor.



The JW7203 will regulate the forward drop across the ORing FET to 25 mV. This is accomplished by controlling the V_{GS} of the MOSFET. As the current decreases the V_{GS} is also decreased, which effectively increases the $R_{DS(on)}$ of the MOSFET. This process is regulated with a low gain amplifier that is gate (ORing FET) pole compensated. The lower gain helps ensure stability over various operating conditions. The regulating amplifier ensures that there is no DC reverse current. However, the amplifier is not very fast and thus it is paired with a fast comparator. This comparator quickly turns off the FET if there is significant reverse current detected.

APPLICATION INFORMATION

Input Power Supply

The power supply for the device is derived from external power through an external current limiting resistor R_{VCC} . R_{VCC} should be sized in such a way to ensure that sufficient current is supplied to the IC at minimum operating voltage corresponding to the falling under voltage threshold. To ensure Stability of internal loop a minimum of 0.1uF is required for C_{VCC} . A 1uF cap is recommended in typical application. To allow for some margin it is recommended that the current through R_{VCC} is at least 1.2x of $I_{Q,MAX}$ when $RTN = Falling$ under voltage threshold and $V_{cc} = 10V$ (minimum recommended operating voltage on VCC). For this example 48V application, R_{VCC} of 16.2k Ω was used. If R_{VCC} is shorted, the external supply voltage should be between 10V and 13.5V. Driving VCC beyond 13.5V may damage the part.

MOSFET Selection

The JW7203 drives N-channel MOSFET to conduct the load current. The important features of the MOSFETs are on-resistance $R_{DS(ON)}$, the maximum drain-source voltage V_{DSS} , and the threshold voltage.

The gate drive for the MOSFET is guaranteed to be greater than 10V and less than V_{cc} . This allows the use of logic level threshold N-channel MOSFET and standard N-channel MOSFET above 10V. An external Zener diode can be used to clamp the potential from the MOSFET's gate to source if the rated breakdown voltage is less than 18V.

The maximum allowable drain-source voltage, BV_{DSS} , must be higher than the supply voltages. If an input is connected to GND, the full supply voltage will appear across the MOSFET.

Input Short-Circuit Faults

The dynamic behavior of an active, ideal diode entering reverse bias is most accurately characterized by a delay followed by a period of reverse recovery. During the delay phase some reverse current is built up, limited by parasitic resistances and inductances. During the reverse recovery phase, energy stored in the parasitic inductances is transferred to other elements in the circuit. Current slew rates during reverse recovery may reach 100A/ μ s or higher.

High slew rates coupled with parasitic inductances in series with the GND and VD paths may cause potentially destructive transients to appear at the GND and VD pins of the JW7203 during reverse recovery. A zero impedance short-circuit directly across an input that is supplying current is especially troublesome because it permits the highest possible reverse current to build up during the delay phase. When the MOSFET finally commutates the reverse current the JW7203 GND pin experiences a negative voltage spike, while the VD pin spikes in the positive direction

R_D Selection

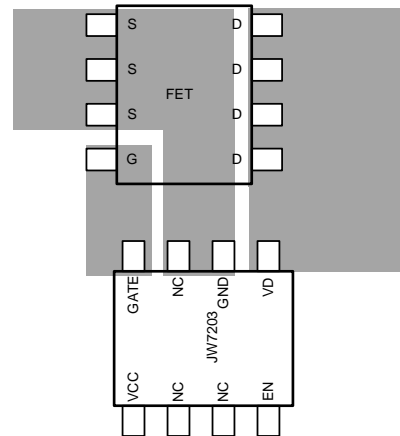
The external resistor R_D is optional, since JW7203 works well without it. To protect VD against negative voltage, it is recommended to add a resistor between VD pin and MOSFET drain. A 100 Ω R_D prevents negative voltage spike of -2V.

PCB Layout Note

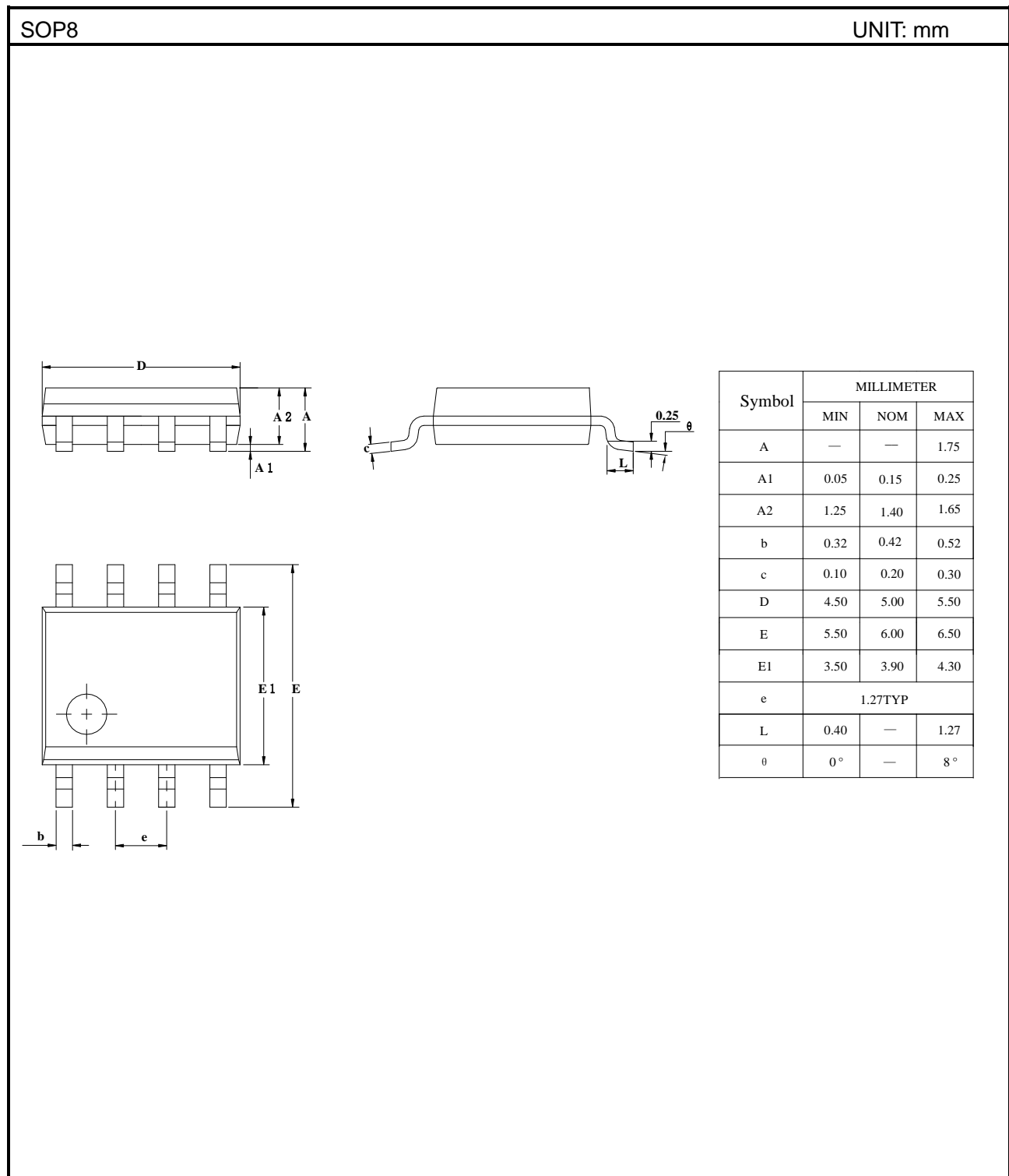
The following advice should be considered when laying out a printed circuit board for the JW7203.

The inputs to the servo amplifiers, VD and GND should be connected as closely as possible to the MOSFET's terminals for good accuracy.

Keep the traces to the MOSFETs wide and short. The PCB traces associated with the power path through the MOSFETs should have low resistance. Use no-clean solder to minimize PCB contamination.



PACKAGE OUTLINE



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