JW7228/JW7228P

100V High-side UV/OV/OC and Reverse Protection Controller with Circuit Breaker

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW®7228 and JW®7228P are high-side protection controllers, JW7228/JW7228P provide intelligent control of a N-channel MOSFET during these applications where the input voltage may be too low, too high or even negative.

JW7228 and JW7228P offer inrush current control to protect MOSFET against system voltage droop and transients. An external capacitor connected from TMR to GND establishes the timeout period to declare a fault condition and Gate is turned off when timeout condition occurs. The under voltage and over voltage protection threshold can be programmed via external resistor dividers. The JW7228 and JW7228P provide automatically restart mode. JW7228P provides PG function, PG keeping high when the voltage of $V_{SNS-VOUT}$ is lower than 1.25V. JW7228P is available in a 10-pin MSOP package and JW7228 is available in a SOP8 package.

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FEATURES

- Wide operating range: 9V to 80V
- Adjustable current limit: 55mV±11%
- Circuit breaker function for severe over-current events
- Internal high side charge pump and gate driver for external N-channel MOSFET
- Adjustable under-voltage lockout (UVLO) and hysteresis
- Adjustable over-voltage lockout (OVLO) and hysteresis
- Initial insertion timer allows ringing and transients to subside after system connection
- Reverse voltage protection support
- Programmable fault timer
- Active high open drain power good output
- Available in automatic restart versions
- Quick output discharge
- Available in 10-pin MSOP package and SOP8 package

APPLICATIONS

- Server Backplane Systems
- Base Station Power Distribution Systems
- Solid State Circuit Breaker
- 24-V and 48-V Industrial Systems

TYPICAL APPLICATION

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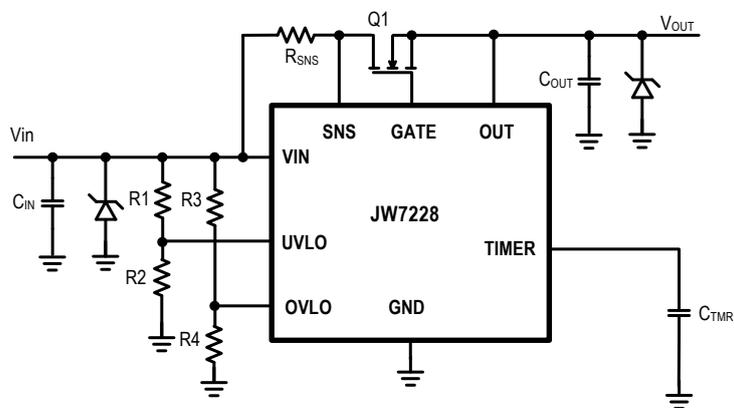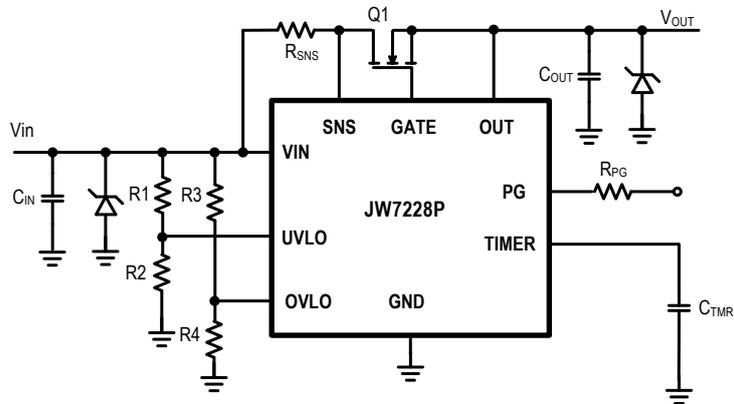
ORDER INFORMATION

DEVICE[1]	PACKAGE	TOP MARKING[2]
JW7228PMSOP#TRPBF	MSOP10	JW7228P YW☐☐☐☐☐
JW7228SOPB#TRPBF	SOP8	JW7228 YW☐☐☐☐☐

Notes：

1) JW☐☐ ☐☐ # TRPBF
   — PB Free
   — Tape and Reel(If"TR"is not shown, it means tube)
   — Package Code
   — Part No.

2) Line1: JW ☐☐☐☐
   — Product code
   — Joulwatt LOGO

   Line2: YW☐☐☐☐
   — Lot number
   — Week code
   — Year code

DEVICE INFORMATION

DEVICE[1]	FEATURE	STATEUS
JW7228PMSOP#TRPBF	Auto-recovery protection mode	Available
JW7228SOPB#TRPBF	Auto-recovery protection mode	Available

PINCONFIGURATION

TOP VIEW

JW7228P

SNS	1		10	GATE
VIN	2		9	OUT
OVLO	3		8	PG
UVLO	4		7	NC
GND	5		6	TIMER

MSOP10

JW7228

SNS	1		8	GATE
VIN	2		7	OUT
UVLO	3		6	TIMER
OVLO	4		5	GND

SOP8
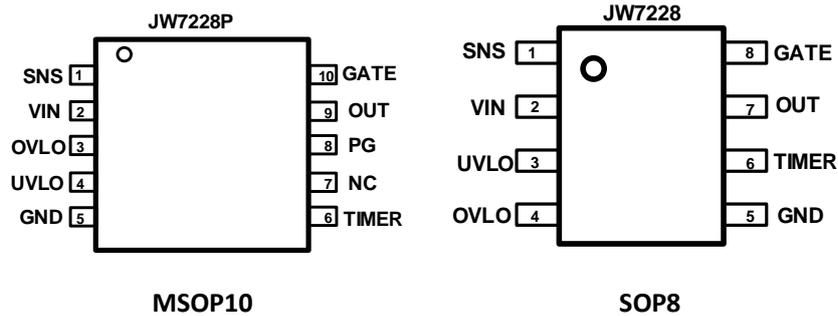
ABSOLUTE MAXIMUM RATING[1]

VIN, SNS, OUT, PG, GATE, UVLO Pins .... -0.3V to 100V
OVLO Pin .... -0.3V to 7V
VIN Pin to SNS Pin .... -0.3V to 0.3V
All Other Pins .... -0.3V to 7V
Junction Temperature[2] …... 150ºC
Lead Temperature ……... 260ºC
Storage Temperature …... -65ºC to +150ºC

RECOMMENDED OPERATING CONDITIONS[3]

Input Voltage VIN   ....9V to 80V
PG Off Voltage ....0V to 80 V
Operating Junction Temperature   ....-40ºC to 125ºC

THERMAL PERFORMANCE[4] θ_{JA} θ_{Jc}

MSOP10...166.5....41.8ºC/W
SOP8...116....54ºC/W

Note：

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.
2) The JW7228/7228P includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB

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ELECTRICAL CHARACTERISTICS

$V_{IN} = 9{\sim}80V$, $T_J = -40ºC{\sim}125ºC$, unless otherwise stated.						
Item	**Symbol**	**Condition**	**Min.**	**Typ.**	**Max.**	**Units**
INPUT (VIN PIN)						
Input current while enable	I_{IN_EN}	UVLO>2.5V and OVLO<2.5V		0.6	1	mA
Input current while disable	I_{IN_DIS}	UVLO<2.5V or OVLO>2.5V		600	800	µA
Power-on reset threshold at VIN to trigger insertion timer	POR_{IT}	VIN increasing		7.6	8	V
Power-on reset threshold at VIN to enable all functions	POR_{EN}	VIN increasing		8.4	9	V
POR_{EN} hysteresis	POR_{EN_HYS}	VIN decreasing		100		mV
OUTPUT (OUTPIN)						
Output bias current , enable	I_{OUT_EN}	OUT = VIN, Normal operation		1.35		µA
Output bias current , disable	I_{OUT_DIS}	Disabled, OUT =0V, SNS=VIN			20	µA
UVLO, OVLO PINS						
UVLO threshold	$UVLO_{TH}$		2.4	2.5	2.6	V
UVLO hysteresis current	$UVLO_{HYS}$	UVLO = 1 V	20	22	30	µA
UVLO delay	$UVLO_{DLY}$	UVLO high delay to GATE high		70		µs
		UVLO low delay to GATE low		11		
UVLO bias current	$UVLO_{BIAS}$	UVLO = 48 V			1	µA
OVLO threshold	$OVLO_{TH}$		2.4	2.5	2.6	V
OVLO hysteresis current	$OVLO_{HYS}$	OVLO = 2.6 V	20	22	30	µA
OVLO delay	$OVLO_{DLY}$	OVLO low delay to GATE high		70		µs
		OVLO high delay to GATE low		11		
OVLO bias current	$OVLO_{BIAS}$	OVLO = 2.4V			1	µA
GATE CONTROL						
Gate source current	I_{GATE}	Normal operation, GATE-OUT =5V	14	19	24	µA
Gate sink current		UVLO < 2.5 V	1.75	2	2.6	mA
		VIN to SNS = 150mV or VIN < POR_{IT}, V_{GATE} = 5 V	140	200	290	mA
Gate output voltage in normal operation	V_{GATE}	GATE-OUT voltage	11	12	13	V
CURRENT LIMIT						
Current limit threshold voltage	V_{CL}	VIN-SNS voltage	48.5	55	61.5	mV
CIRCUIT BREAKER						
Circuit breaker threshold	V_{CL}	VIN-SNS voltage	80	105	130	mV

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$V_{IN} = 9{\sim}80V$, $T_J = -40ºC{\sim}125ºC$, unless otherwise stated.						
Item	**Symbol**	**Condition**	**Min.**	**Typ.**	**Max.**	**Units**
voltage						
Circuit breaker response time	t_{CB}	VIN-SNS stepped from 0 mV to 80 mV		0.5	1.2	μs
TIMER (TIMER PIN)						
TIMER upper threshold	V_{TMRH}		3.7	3.93	4.16	V
TIMER lower threshold	V_{TMRL}	Restart cycles	1.15	1.23	1.31	V
		End of 8th cycle		0.3		V
		Re-enable Threshold		0.3		V
Insertion time current			4	6	8	μA
Sink current , end of insertion time	I_{TMR}	TIMER pin = 2 V	1	1.5	2	mA
Fault detection current			70	95	120	μA
Fault sink current			1.25	2.5	3.75	μA
Fault restart duty cycle[5]	DC_{Fault}			0.5%		
POWER GOOD (PGPIN)						
Power good threshold measured at SNS-OUT	PG_{TH}	Decreasing (JW7228P)	0.67	1.25	1.85	V
		Increasing, relative to decreasing threshold (JW7228P)	0.95	1.25	1.55	
PG output low voltage	PG_{VOL}	I_{SINK} = 2 mA (JW7228P)		60	150	mV
PG off leakage current	PG_{IOH}	V_{PG} = 80 V (JW7228P)			1	μA

Note：

5) Guaranteed by design.

PIN DESCRIPTION

Pin MSOP10	Pin SOP8	Name	Description
1	1	SNS	Current sense input. Used to measure current and regulate it. Kelvin sense is necessary to ensure accurate current limits
2	2	VIN	Input sense and power supply
4	3	UVLO	Under-voltage lockout. Under voltage protection threshold and hysteresis can be programmed via external resistor divider.
3	4	OVLO	Over-voltage lockout. Over voltage protection threshold and hysteresis can be programmed via external resistor divider.
5	5	GND	Ground.
6	6	TIMER	Timing set pin. The fault timeout period is programmed by an external capacitor connected from this pin to GND.
7	-	NC	Not be connected. The pin can't be connected to GND.
8	-	PG	Active high. An open drain power good indicator.
9	7	OUT	Output feedback. Used to measure the voltage across the MOSFET.
10	8	GATE	Gate driver output for external MOSFET

BLOCK DIAGRAM

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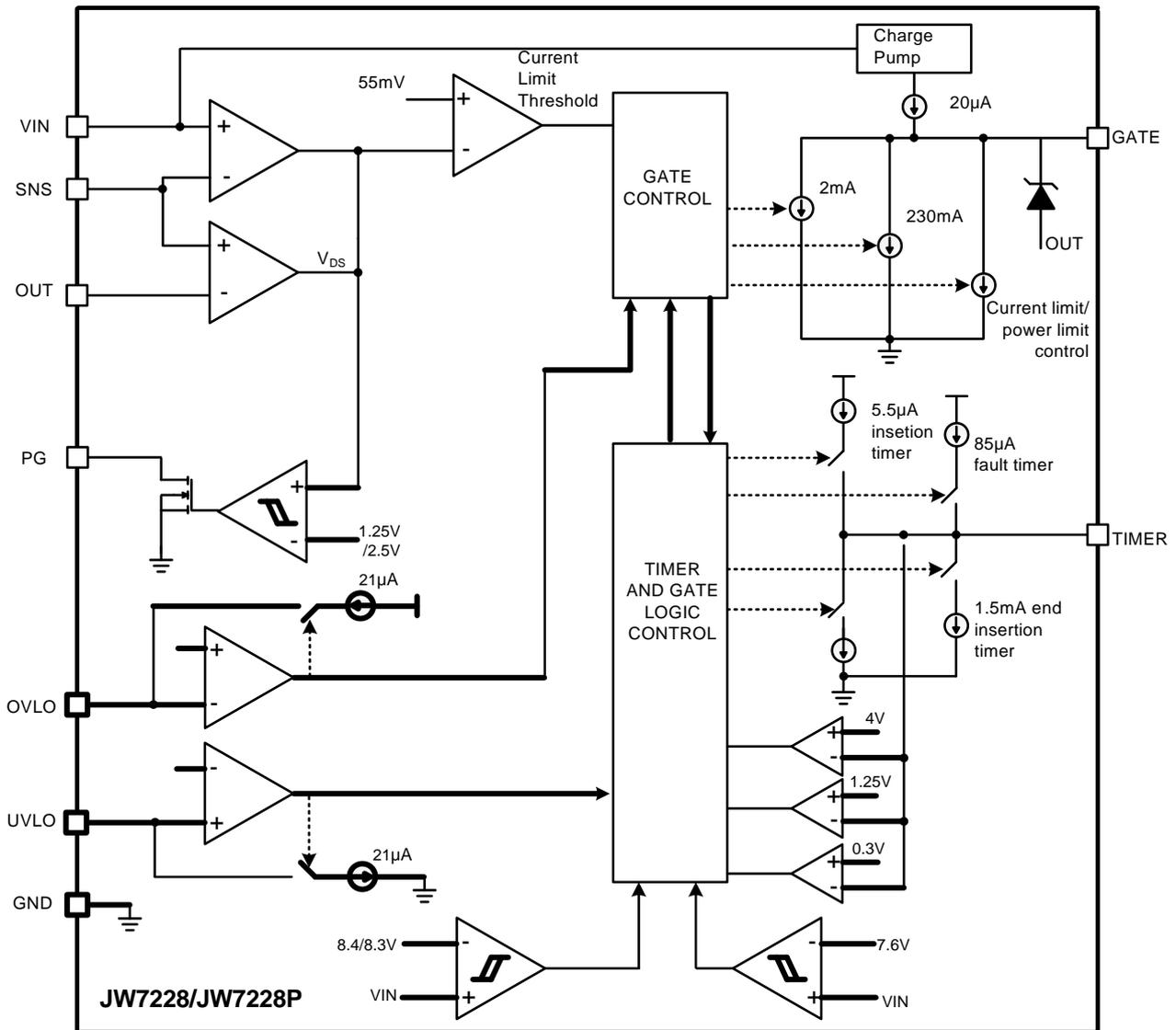
FUNCTIONAL DESCRIPTION

The JW7228 and JW7228P are high-side protection controllers, JW7228/JW7228P provide intelligent control of a N-channel MOSFET during these applications where the input voltage may be too low, too high or even negative.

Power Up Sequence

As initially increases, the gate of external N-channel MOSFET is pull down by 230mA current. The 230mA pull down current prevents an inadvertent turn-on as the Miller capacitor of external MOSFET is charged. Additionally, the TIMER pin is initially pull down to GND until VIN reaching POR_{IT} threshold. During the insertion time (t_1), the gate of external MOSFET is held off by 2mA sinking current and TIMER pin is charged by 5.5uA sourcing current. The insertion time prevent MOSFET turn-on while VIN ringing and transients. The insertion time will continue until the voltage of TIMER reaching 4V then C_{TMR} is pull down by 1.5mA sinking current. The duration of insertion time can be computed using equation below:

$$t_{insertion\_time} = \frac{C_{TMR} \times 4V}{5.5\mu A}$$

After the insertion time, the JW7228 and JW7228P control circuitry is enabled when VIN reaches the POR_{EN} threshold. The GATE pin is turned on when the voltage of UVLO exceeds the UVLO threshold (2.5V) and the inrush time (t_2) is beginning.

The GATE of external MOSFET is charged by 20μA souring current and the maximum V_{GS} voltage is clamped below 12V by internal circuit.

During the inrush time, the inrush current is limited by current limit. An internal 85μA sourcing current charges C_{TMR} while current limit is active. If the current of MOSFET reduce

below limiting threshold before the voltage of TIMER reaching 4V, the inrush time ends and 85μA sourcing current is switched off, then C_{TMR} is discharged by 2.5μA sinking current. If the current limit is still active when the voltage of C_{TMR} reaches 4V. A fault condition is declared and the external MOSFET is turned off. JW7228 and JW7228P enter into retry mode. To avoid timeout during inrush time, C_{TMR} can be computed by below equation:

$$C_{TMR} \geq \frac{t_{inrush\_time} \times 85\mu A}{4V}$$
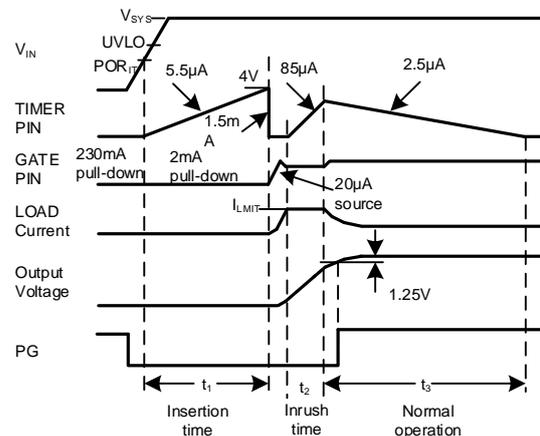
Figure 1. Power-Up Sequence (Current Limit Only)

GATE Control

A charge pump sources 20μA to enhance the external MOSFET. The voltage between GATE to source is limited by internal clamp circuit. The gate of external MOSFET is held charged by 20μA sourcing current to approximately 12V above OUT during normal operation time (t_3). An external Zener diode is recommended if the maximum VGS rating of the external MOSFET is less than 12V. The forward current rating of the external Zener diode should be larger than 250mA.

When the system voltage is initially applied, the GATE pin is held low by a 230mA pull-down

current. This helps prevent an inadvertent turn-on as the Miller capacitor of the external MOSFET is charged.

During the insertion time (t_1) the GATE is keeping pull down by 2mA sinking current. The external MOSFET is hold off until the end of t_1. During the inrush time (t_2), the GATE voltage is modulated to regulate the current or power dissipation level.

If the current limit is still active when the voltage of C_{TMR} reaches 4V. The GATE is pull down by 2mA current. A fault condition is declared. If the current of MOSFET reduce below limiting threshold before the voltage of TIMER reaching 4V, The GATE is held charging and JW7228 and JW7228P enters normal operating time.

If under voltage protection or over voltage protection is triggered, the GATE pin is pulled low by the 2mA pull-down current to turn off the external MOSFET.
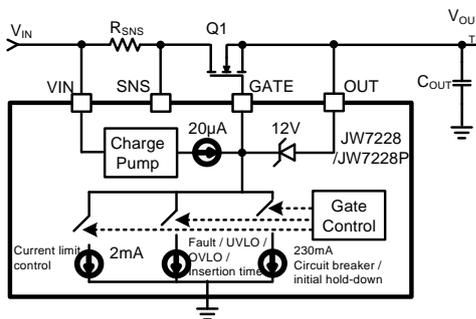
Figure 2. GATE Control

Fault Timer and Restart

If the current limit is still active when the voltage of TIMER reaches 4V, the GATE is held off by 2mA current.
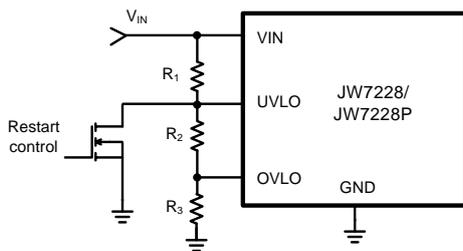
Figure 3. Restart Control

The JW7228 and JW7228P enter automatic restart sequence. The TIMER pin continues to charge and discharge between 1.25V and 4V seven times as shown in Figure 4. During restart sequence, the C_{TMR} charging current is 85µA while discharging current is 2.5µA. When the TIMER pin reaches 0.3V during the eighth high to low ramp, the 20µA current sourcing at the GATE pin turns on external MOSFET. If the fault condition is not removed, the timeout period and the restart cycle repeat.
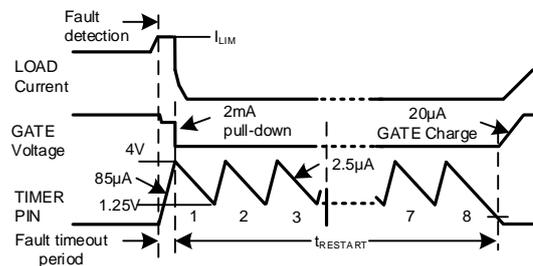

Figure 4. Restart Sequence

Shutdown Control

The external MOSFET can be remotely turned off by pull UVLO pin low or pull OVLO pin high. Both UVLO and OVLO threshold is 2.5V. Typical application is shown as Figure 5.
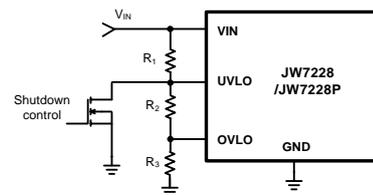

Figure 5. Shutdown Control

Current Limit

The load current is measured by the voltage between VIN and SNS. The current limit protection is active when the voltage across the sense resistor R_{SNS} reaches 55mV. In the current limit condition, the GATE is modulated to regulate the voltage across R_{SNS} around 55mV and C_{TMR} is charged by internal 85µA sourcing current. If the load current decrease

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below 55mV before the voltage of TIMER reaching 4V, IC recover to normal operation mode. The R_{SNS} resistor is recommended to be smaller than 100 mΩ.

Circuit Breaker

The JW7228 and JW7228P incorporate two distinct thresholds: a current limit threshold (55mV) and a fast-trip threshold. The fast-trip threshold protects the system against a serve over load and hot short circuit. When the voltage across the sense resistor R_{SNS} exceeds the 105mV fast trip threshold, the GATE pin immediately pulls the external MOSFET gate to ground with approximate 230mA, and a fault time-out period begins. When the voltage across R_{SNS} falls below 105 mV, the 230mA pull-down current at the GATE pin is switched off, and the gate voltage of external MOSFET is then modulated to regulate load current.

Power Limit Protection

JW7228 and JW7228P have extra built-in power limit protection for the better utilization of external MOSFET's SOA. The power limit is constant and works when V_{DS} is over 21.7V. The power limit can be calculated by multiplying the V_{DS} (V_{SNS}-V_{OUT}) of the external MOSFET and the voltage across R_{SNS}. The power limit can be calculated using following equation:

$$P_{LIMIT}（W）= \frac{1192(V^2)}{R_{SNS}(m\Omega)}$$
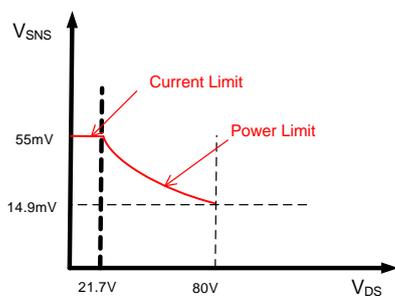
Figure 6. The Curve Reflecting Power Limit

Under-voltage Lockout (UVLO)

Both threshold and hysteresis can be programmed for under voltage protection. The UVLO rising threshold is set by R_1 and R_2 (shown in Figure 7) according to below equation:

$$UVLO_{rising} = \frac{R_1 + R_2}{R_2} \times 2.5V + R_1 \times 21\mu A$$

The hysteresis of UVLO is shown below:

$$UVLO_{hyst} = R_1 \times 21\mu A$$

The UVLO pin sinks 21µA current when VIN is below UVLO$_{rising}$. When VIN rise up above UVLO$_{rising}$, the 21µA sinking current is switched off and GATE is pull up by 20µA if the insertion time is finished. In general, the rising UVLO threshold should be sufficiently below the minimum input voltage.
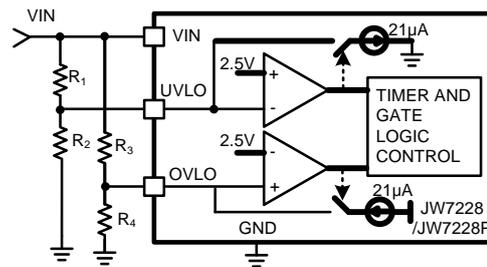
**Figure 7. UVLO and OVLO Thresholds Set By R1-R3**

Over-voltage Lockout (OVLO)

Both threshold and hysteresis can be programmed for over voltage protection. The OVLO rising threshold is set by R3 and R4 (shown in Figure 7) according to below equation:

$$OVLO_{falling} = \frac{R_3 + R_4}{R_4} \times 2.5V - R_3 \times 21\mu A$$

The hysteresis of OVLO is shown below:

$$OVLO_{hyst} = R_3 \times 21\mu A$$

The OVLO pin sources 21µA current when VIN is above OVLO$_{rising}$. When VIN falling down below OVLO$_{falling}$, the 21µA sourcing current is switched off and GATE is pull up by 20µA if the insertion time is finished. In general, the falling

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OVLO threshold should be sufficiently above the maximum input voltage.

Power Good Indicator

The Power Good pin is an open drain indicator. Before insertion time, when VIN increases above 5V, PG switches low. PG keeps low until the voltage of OUT pin increases to V_{SNS}-1.25V (V_{DS}<1.25V). The PG pin keeps high until the drain-source voltage of the external MOSFET is above 2.5V. A pull up resistor (R_{PG}) is recommended as shown in Figure 8. It's critical to keep the downstream DC/DC off while the controller is charging the bulk capacitor. This can be accomplished through the PG pin.
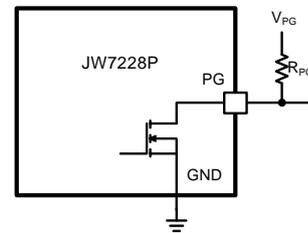

Figure 8. Power Good Output

APPLICATION INFORMATION

The JW7228 and JW7228P are UV/OV/OCP and reverse protection controllers for 12~72V system application and is used to manage inrush current and protect downstream circuitry and upstream bus in case of fault condition.

Typical Application
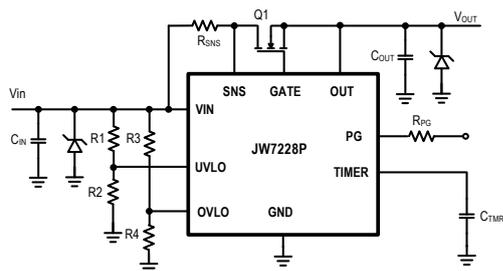
Figure 9. Typical Application

When the input supply is plugged in backwards, or a negative supply is inadvertently connected, the JW7228/JW7228P provide the reverse supply protection with an external back to back N-channel MOSFETS and a diode connecting the GND of JW7228/JW7228P and the GND of power source.
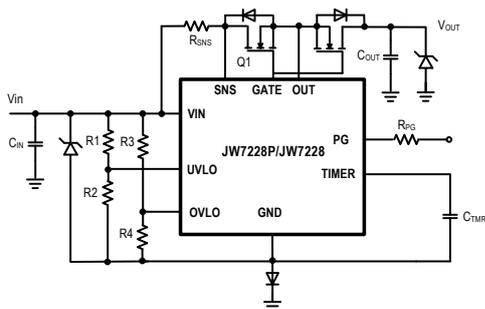

Figure 10. Application with Reverse Supply Protection

UVLO and OVLO Setting

Both the threshold and hysteresis can be programmed by external resistor divider. Usually the rising UVLO threshold should be set sufficiently below the minimum input voltage and the falling OVLO threshold should be set sufficiently above the maximum input voltage.

For this example, UV rising threshold is 14V and UV falling threshold is 12V. R_1 can be chosen according to 2V UV threshold.

$$R_1 = \frac{UV_{hyst}}{21\mu A} = \frac{2V}{21\mu A} = 95k\Omega$$

R_2 can be computed by equation shown as

$$R_2 = \frac{R1}{UV_{rising} - 2.5V} = \frac{95k\Omega}{14 - 2.5} \times 2.5 = 20.6k\Omega$$

The OV setting can be programmed as a similar fashion as shown in equations below

$$R_3 = \frac{OV_{hyst}}{21\mu A} = \frac{2V}{21\mu A} = 95k\Omega$$

$$R_4 = \frac{R_3}{OV_{falling} - 2.5V} = \frac{95k\Omega}{38 - 2.5} \times 2.5 = 6.69k\Omega$$

Choose available value as R_1=R_3=100kΩ, R_2=20kΩ, R_4=6.8kΩ.

PCB Layout Note

For minimum noise problem and best operating performance, the PCB is preferred to following the guidelines as reference.

1. VIN pin and SNS pin need to have a Kelvin Sense connection to the sense resistor R_{SNS}.
2. Keep the decoupling capacitor on VIN pin as close to the IC as possible.
3. A Shottky diode is recommended to be connected from GND to OUT pin.
4. A large voltage can develop between VIN and SNS, if the bypass capacitor is placed right next to the pin and the trace from RSNS to the pin is long, a LC filter is formed. This could result in a violation of the ABS max rating from VIN to SNS.
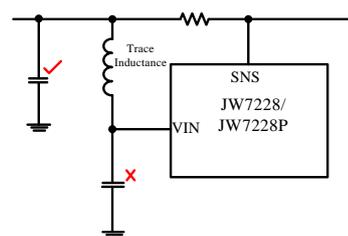

Figure 11. PCB Layout Note

PACKAGE OUTLINE

MSOP10	UNIT: mm

Symbol	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.10
A1	0.02	—	0.15
A2	0.75	—	0.95
b	0.18	—	0.33
c	0.09	—	0.23
D	2.90	3.00	3.10
E	4.75	—	5.05
E1	2.90	—	3.10
e	0.50(BSC)		
L	0.40	—	0.80
θ	0°	—	8°

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE

Sprocket Holes

Procket Quadrants

Package Type	Pin1 Quadrant
MSOP10	1

SOP8   UNIT: mm

Symbol	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.05	0.15	0.25
A2	1.25	1.40	1.65
b	0.32	0.42	0.52
c	0.10	0.20	0.30
D	4.50	5.00	5.50
E	5.50	6.00	6.50
E1	3.50	3.90	4.30
e	1.27TYP		
L	0.40	—	1.27
θ	0 °	—	8 °

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE

Sprocket Holes

Procket Quadrants

Package Type	Pin1 Quadrant
SOP8	1

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